ALCHIP MINIMIZES DYNAMIC POWER FOR HIGH-PERFORMANCE COMPUTING ASICS

HIROYUKI FURUZONO, ALCHIP TECHNOLOGIES, LIMITED

RTL LOW-POWER WHITEPAPER

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INTRODUCTION

Headquartered in Taiwan, Alchip® is a fabless ASIC provider that delivers turnkey solutions that support IC design, testing, prototyping, and mass-production utilizing leading-edge process technologies. We help customers creating applications in the consumer, automotive, and high-performance computing markets.

With a focus on high-performance computing ASICs, our team decided to undertake a new project where we would employ the PowerPro® RTL Low-Power Platform to reduce dynamic power consumption within our unique fishbone clock tree methodology. Could we achieve better power results using PowerPro and could we integrate the tool within our team and the existing design flow? This whitepaper documents our journey and the successful results of the project.

UNDERSTANDING FISHBONE CLOCK TREES AND THE DESIGN

The traditional clock tree synthesis (CTS) methodology is aptly-named, as the buffered datapaths look like tree branches. An RTL synthesis tool adjusts the buffer delays based on the flip-flop distribution. The fishbone clock design methodology balances the stage count from the root to all the flip-flops by employing multi-drivers in a pattern that resembles the bones within a fish. Figure 1 shows the conceptual differences between the two methodologies.

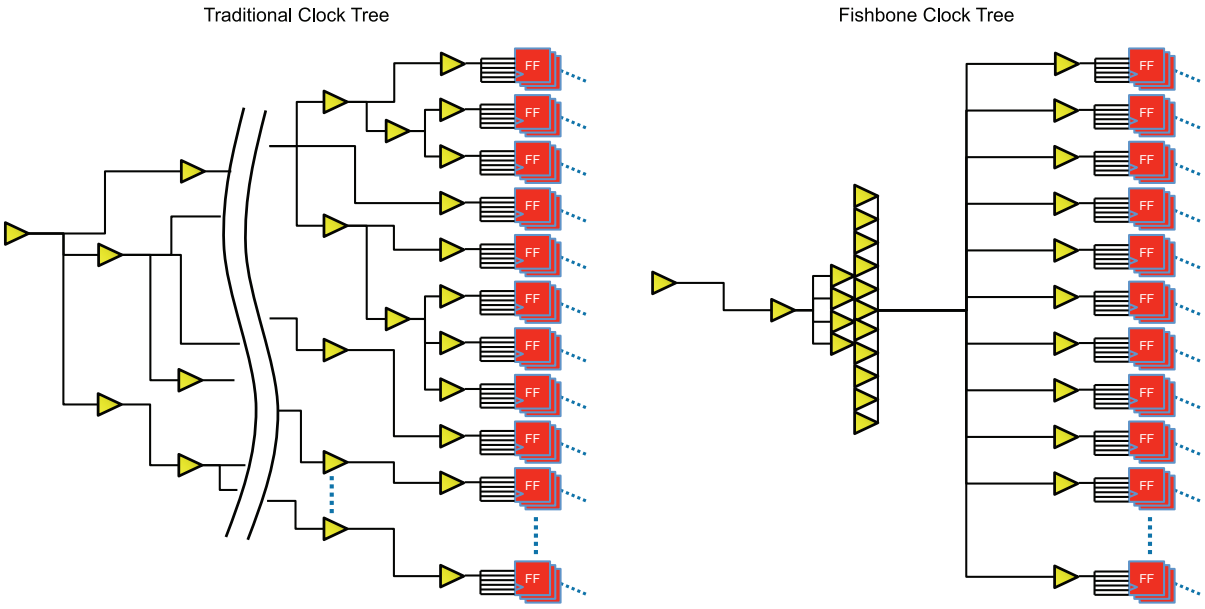

Figure 1: Clock tree methodology comparison

For high-performance computing ICs, the clock frequency of the CPU can reach 2GHz and the power consumption of the clock network can contribute up to 70% of the total dynamic power consumption. We have found that the fishbone clock tree methodology is the key for power reduction compared to traditional CTS (Table 1).

	Traditional CTS	Alchip Fishbone
Clock buffer stages	10-20 stages	2-3 stages
Clock network area	Occupies significant routing resource	10-25% savings of clock buffer area
Insertion delay	> 500ps	< 200ps
Skew control	• < 50ps (tool only) • CTS skew significantly increased with on-chip variation effect added • Very large number of hold time violations	• < 50ps (tool & silicon) • Possible single corner hold time closure (less variation)
Uncertainty (design margin)	Large design margin	No over-design
Power dissipation	• Large number of clock buffers • Large number of hold buffers • Over-design introduces more power consumption • Large clock network capacitance	• Fewer clock buffers • Fewer hold buffers • Consistency with silicon • Lower clock network capacitance

Table 1: Traditional CTS is less favorable than the Alchip Fishbone methodology

The specifications for the actual high-performance computing design project include:

- Specific-purpose super computer
- Core processor: 24 x 24 array structure
- 16nm technology process
- 600 MHz clock frequency

In order to reduce dynamic power for the project, we concentrated on:

- Low-power clock design methodology
- Clock gating
- Memory gating

Our questions at the start of the project were: will PowerPro support our fishbone methodology and will the tool improve dynamic power consumption?

INTRODUCING THE POWERPRO LOW-POWER PLATFORM

The PowerPro RTL Low-Power Platform provides a complete solution to accurately measure, interactively explore, and to optimize power during the RTL development cycle. Using PowerPro, designers can evaluate power consumption directly on the RTL design rather than going through the time-consuming steps of physical implementation. PowerPro's physical-aware flow provides the necessary accuracy for the estimated power values of the design.

Throughout the RTL development process, the power exploration flow provides guidance on where power is wasted and how to reduce it. PowerPro provides many micro-architectural and fine-grained optimization

possibilities for the design and it presents the actual power savings associated with each change. This interactive, "what-if?" analysis allows designers to quickly assess the impact of changes on the design.

Because our team was focused on clock gating, we concentrated on sequential clock gating optimization and memory gating optimization within PowerPro.

SEQUENTIAL CLOCK GATING OPTIMIZATION

Sequential clock gating has a big impact on power savings because it shuts off registers and the datapath logic driven by those registers to reduce switching activity. Normally, sequential clock gating requires an experienced engineer to analyze the sequential behavior of the design over multiple clock cycles to decide what registers can be gated and under what enable conditions. PowerPro automates this process by performing sequential analysis over many clock cycles. Figure 2 shows a typical approach for adding a clock gate (CG) for a register that a logic synthesis tool might utilize.

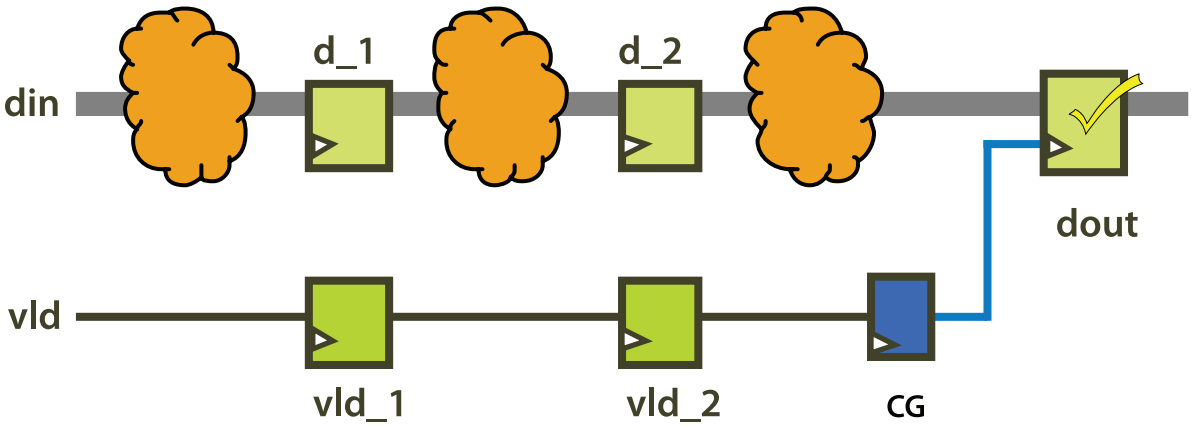

Figure 2: Typical logic synthesis tool clock gate

PowerPro finds new enable conditions, using advanced sequential analysis, and adjusts the design (Figure 3). This technique is called Observability-Based Sequential Clock Gating. The red checkmarks indicate additional gating due to enables inserted by PowerPro.

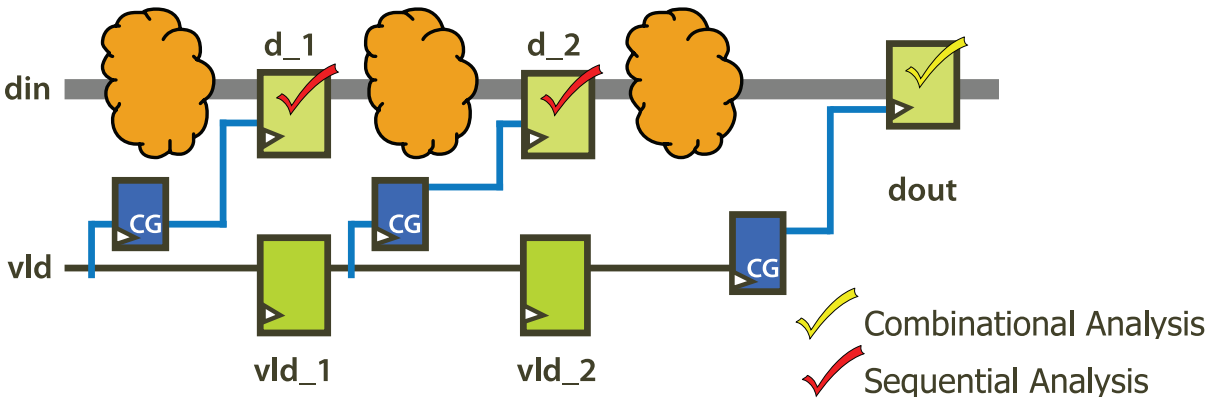

Figure 3: PowerPro employs Observability-Based Sequential Clock Gating

Another type of clock gating employed by the team is called Input Stability-Based Sequential Clock Gating. For example, Figure 4 shows the original RTL logic for a datapath.

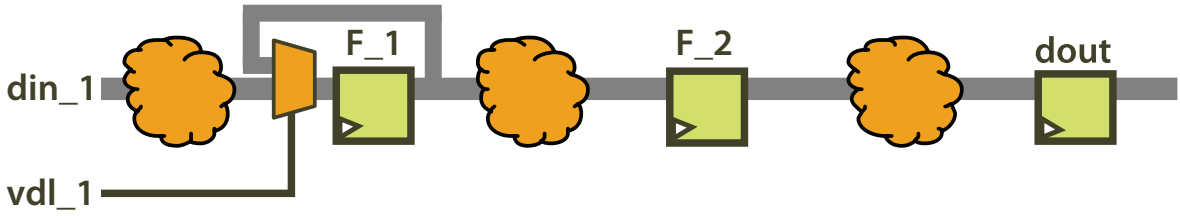

Figure 4: Original RTL logic before analysis

Figure 5 shows the results of the PowerPro analysis. The yellow checkmarks show combinational clock gating opportunities which a logic synthesis tool might be able to realize. However, the red checkmarks indicate clock gating opportunities that PowerPro uniquely discovers. The tool generates the sequential enable signals for all the opportunities and they are eventually moved to the corresponding clocks by the logic synthesis tool during the process of insertion of the integrated clock gating cells.

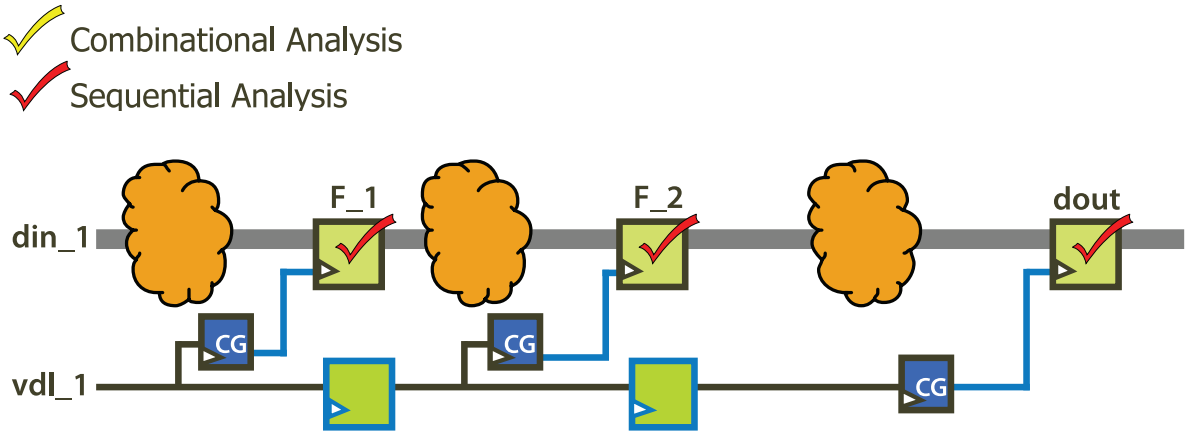

Figure 5: PowerPro discovers additional clock gating opportunities

MEMORY GATING OPTIMIZATION

Removing redundant memory accesses can result in significant reduction in the dynamic power consumption of memories. PowerPro memory gating can automatically analyze a design for conditions under which the value read out of a memory is not used by the downstream logic. The tool then adds logic to the memory enable to disable such redundant reads. This transformation is called Observability-Based Read Gating. Figure 6 shows the observability-based gating condition propagated across one level of sequential logic. But in more complex designs, such conditions can propagate across multiple levels of sequential logic and generate gating conditions to shut off redundant memory reads, thereby saving dynamic power in the memory.

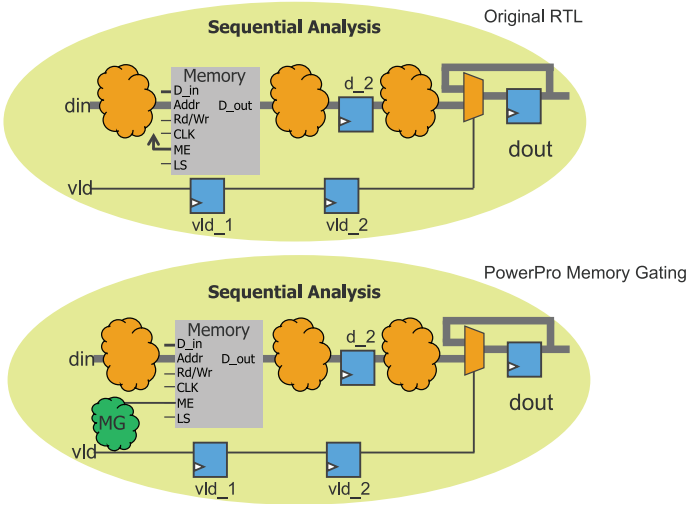

Figure 6: Observability-Based Read Gating

Many memories are read more often than they are written. One example is a memory of coefficients that are used in a digital filter. In these memories, the same address can be repeatedly read without any intervening writes. In such a scenario, all the reads to the same address of the memory after the first one are redundant and can be gated. This transformation is referred to as Stability-Based Read Gating because it relies on the stability of the read address and read enable of the memory to gate off redundant reads. Figure 7 illustrates this concept.

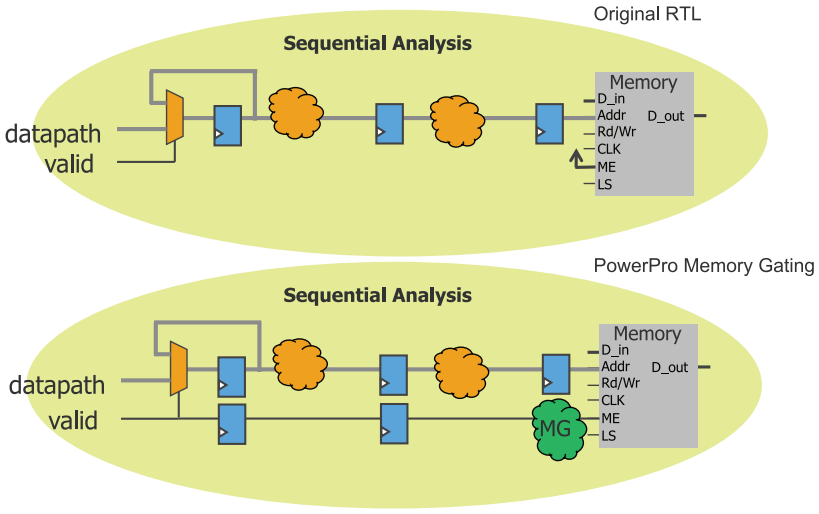

Figure 7: Stability-Based Write Gating

ADDING POWERPRO TO THE FLOW

We added PowerPro to our existing design flow (Figure 8). This required supporting input data for the tool.

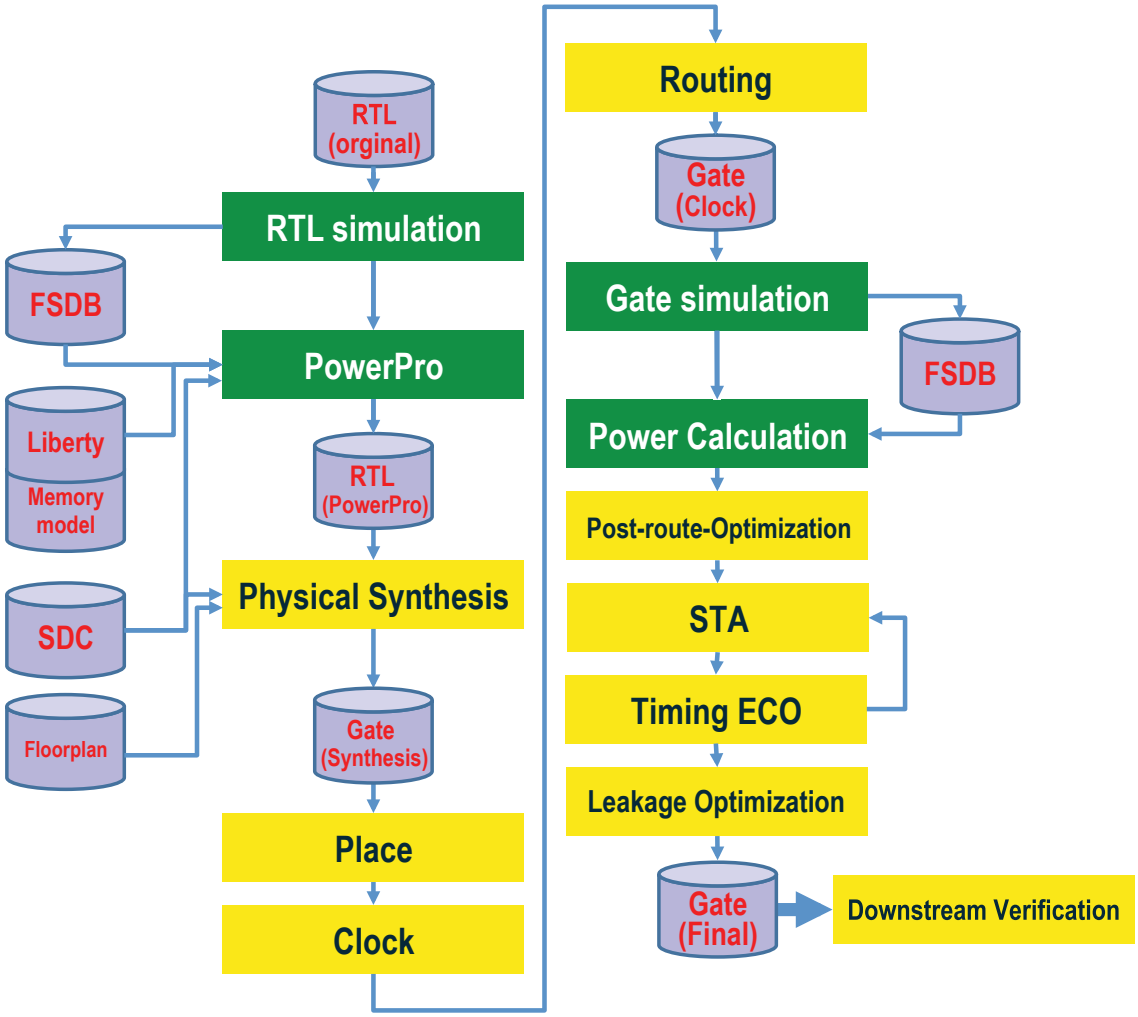

Figure 8: Adding PowerPro to the existing design flow

The RTL simulation captures the Fast Signal Database (FSDB) representing the simulator signal patterns. That information is an input to PowerPro, along with the Liberty™ format. The Liberty™ format is maintained by Synopsys and it is an open-source library used for modeling gate-level timing and power. Alchip supports wrapper level SRAM model generation that instance multiple SRAM macro instances. This memory model is required as an input to PowerPro to support memory gating.

Using the FSDB from the gate-level simulation after placement and routing, we could calculate the actual power results and compare those to the estimated power from the RTL that PowerPro calculated.

EXAMINING THE RESULTS

Table 2 shows the PowerPro report data comparing the power consumption of the RTL design before using the tool and after. The PowerPro techniques resulted in the flip-flop (FF) power being reduced by 26% and the memory power was reduced by 80%.

	After PowerPro (mW)			Before PowerPro (mW)		
	Dynamic	Static	Total	Dynamic	Static	Total
FF	3.978	0.450	4.429	5.565	0.449	6.014
Memory	8.449	0.860	9.309	44.922	0.860	45.783

Table 2: RTL power results

After moving the design through the place and route steps in the design flow, we captured the post-layout results and compared the power savings created by PowerPro. We also compared the design using the fishbone architecture against the traditional clock tree synthesis methodology (Table 3).

		With/ PowerPro (ratio)			Without/ PowerPro (ratio)		
		Dynamic	Static	Total	Dynamic	Static	Total
Fisbone	Clock	30.2	19.2	30.0	34.6	10.6	34.3
	FF	60.5	100.1	70.0	101.2	100.0	100.9
	Combinational	39.6	98.5	56.1	101.2	100.0	100.9
	Memory	12.8	100.0	14.2	100.0	100.0	100.0
	Total	30.0	97.7	41.0	90.0	99.0	91.5
CTS	Clock	95.5	110.0	95.7	100.0	100.0	100.0
	FF	59.4	100.1	69.1	100.0	100.0	100.0
	Combinational	38.2	98.5	55.1	100.0	100.0	100.0
	Memory	12.8	100.0	14.2	100.0	100.0	100.0
	Total	39.9	98.9	49.5	100.0	100.0	100.0

Table 3: Post-layout results

Table 3 points out some of the success of using the new design flow, including:

1. The effect of the fishbone architecture combined with using PowerPro reduces the total power of the design by 59%.
2. Comparing the CTS versus the fishbone architecture when using PowerPro shows that the clock network power is reduced by 69%.
3. Comparing the total power between the fishbone design with and without using PowerPro shows that PowerPro lowered the total power 55%, the flip-flop power by 31%, and the memory power 86%. This correlates well with the PowerPro estimate at the RTL design level (before layout) of 26% flip-flop and 80% memory power reduction, which was conservative.

Clock network power could be reduced drastically because of the significant buffer count and capacitance reduction with fishbone architecture. Table 4 shows the buffer count and capacitance comparison result.

	Fishbone		Conventional CTS	
Buffer Count	219	10.7%	2047	100.0%
Pin capacitance (pF)	6.5	34.9%	18.6	100.0%
Wire capacitance (pF)	11.8	38.6%	30.6	100.0%

Table 4: Fishbone clock shows the significant benefit for power reduction

At the conclusion of our project, we also analyzed the clock and memory gating effectiveness. Table 5 shows that PowerPro adds more gating cells and the flip-flop gating ratio in the design increased 68.18%.

	With PowerPro		Without PowerPro	
	# of cells	%	% of cells	%
Clock Gating	2238	---	1752	---
Gated FF	28491	68.18%	22168	53.33%
Un-Gated FF	13295	31.82%	19402	46.67%
Total FF	41785	100.00%	41571	100.00%

Table 5: PowerPro increases the clock gating ratio

The clock gating cells added did not cause negative effects in the design and the higher gating ratio decreased the average toggling percentage on the output of the integrated clock gating (ICG) as Figure 9 shows.

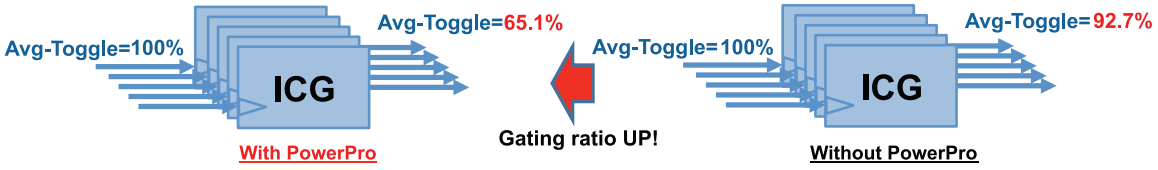

Figure 9: Decreased average toggling after clock gating

To maintain RTL code portability, the SRAM enable was intentionally not controlled. This represented the worst-case power consumption scenario for memories. PowerPro automatically detected the enable control signal and gated the SRAM appropriately, leading to a significant reduction of power consumption, as Table 6 shows.

	With PowerPro (mW)			Without PowerPro (mW)		
	Dynamic	Static	Total	Dynamic	Static	Total
Memory	8.449	0.860	9.309	44.922	0.860	45.783

Table 6: PowerPro memory gating significantly reduces power consumption

PUTTING THE SOLUTION INTO PRACTICE

Because we are a fabless ASIC company, we support PowerPro within our customer's design flow. The customer runs the PowerPro flow and provides the power-optimized RTL to us. We then focus on the layout and backend flow. We can also customize this customer interface model on a case-by-case basis. Within this interface model (Figure 10), we depend on Mentor for PowerPro support.

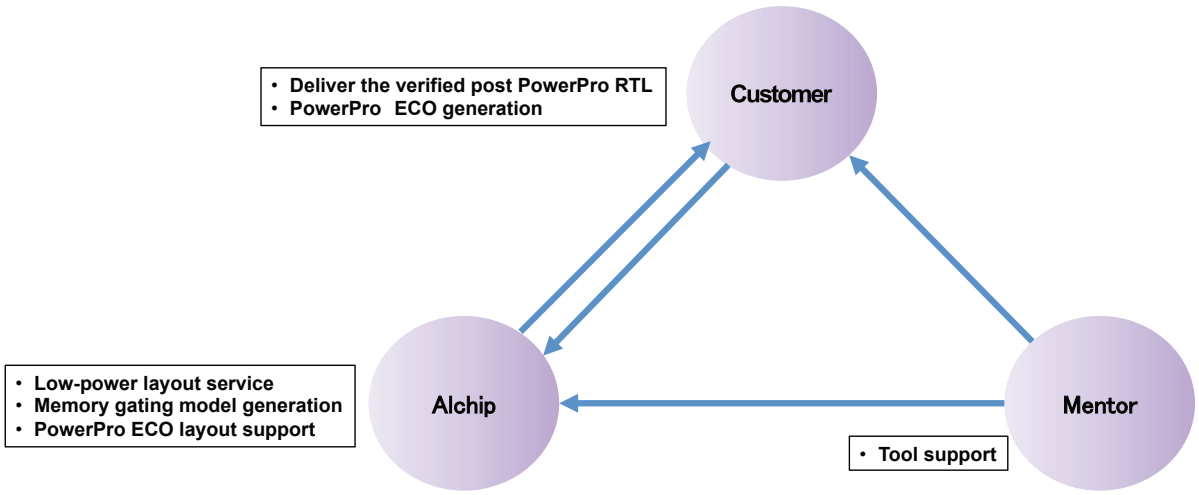

Figure 10: The customer interface model

We also support the ability for the customer to make an engineering change order (ECO) by leveraging the ECO flow that PowerPro supports. ECOs often arrive after synthesis, while the design is being placed and routed, or while the design is being iterated between synthesis and layout. ECOs usually disrupt the design flow, causing designers to lose much of the previous iteration work on the design to make it meet performance, area, and power constraints. The ECO flow in PowerPro provides an alternative way to validate the already-implemented gates in order to avoid resynthesizing a stable design that has already undergone layout and timing analysis.

OUR NEXT STEPS

We started this project with the questions: "Could we achieve better power results using PowerPro and could we integrate the tool within our team and the existing design flow?" We have answered that question positively with better power results using the tool and the seamless support of our fishbone architecture. We consider PowerPro as a powerful tool within our low-power methodology. We believe that PowerPro will be very useful for the other types of designs that we specialize in, beyond high-performance computing ASICs, and we plan to proactively adopt PowerPro on our new 7nm process.

To learn more about the PowerPro RTL Low-Power Platform, see the website here.

For the latest product information, call us or visit: www.mentor.com

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

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