HyperLynx DRC Free Edition

DATASHEET

Overview

HyperLynx® DRC is a FREE, powerful, fast, electrical design rule checking tool that can automate the verification process and save hours of manual inspection. Available in several configurations, HyperLynx DRC allows for verification of complex design rules that are not easily simulated, such as rules for traces crossing splits and EMI/EMC.

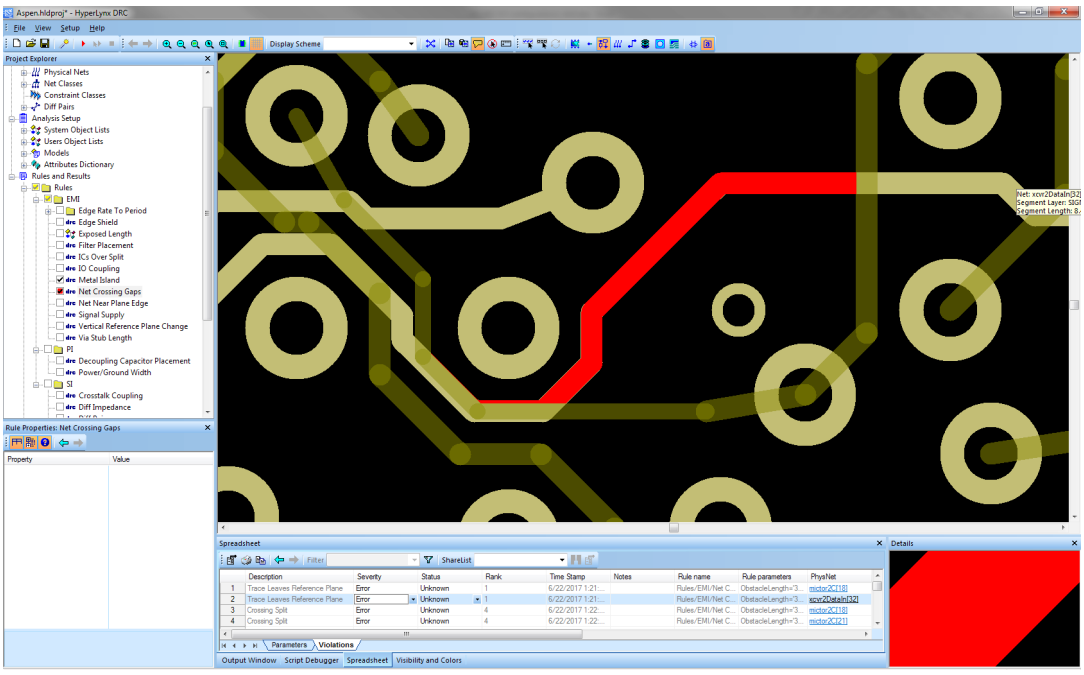
What's Included

With eight standard Design Rule Checks (DRCs) for items such as traces crossing splits, T-fork topology, and decoupling capacitor placement, the HyperLynx DRC Free Edition lets you quickly and easily pinpoint trouble spots on your board that can cause issues with signal integrity (SI), power integrity (PI), and electromagnetic interference and compliance (EMI/EMC).

Built-in engines for geometric calculation, path finding, and net topology extraction, along with a 2D field solver, provide quick and accurate results without the need for preparing device models.

FEATURES AND BENEFITS:

- Eight built-in design checks for SI, EMI/EMC, and PI
- No-cost annual subscription
- Rule parameters can be edited based on technology or corporate guidelines
- Advanced geometric engine for powerful and efficient design rule checking
- Easy setup and navigation
- Automatically generated HTML error report
- Support for all PCB layout formats
- Add more rules with HyperLynx DRC Gold or Developer editions



HyperLynx DRC performs electrical Design Rule Checks on boards for EMI/EMC issues, as well as Signal Integrity and Power Integrity. Automated net filtering suppresses false violations.

Easy Setup and Navigation

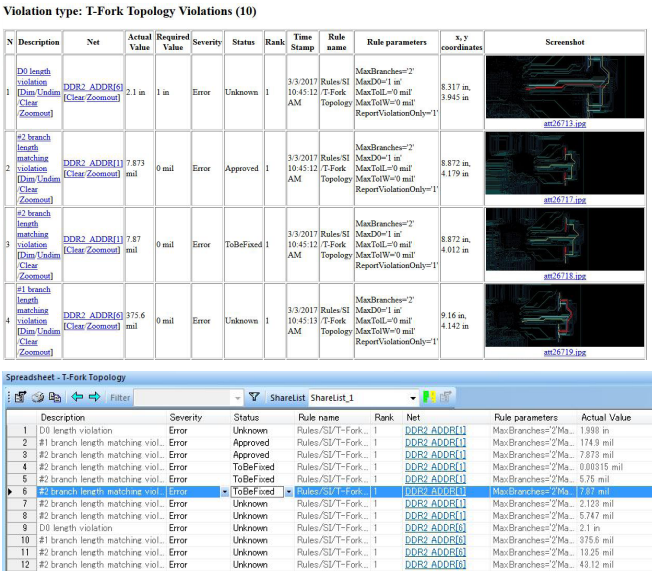
The HyperLynx DRC Free Edition is designed for quick and easy access to design data. A built-in Setup Wizard walks you through the steps for running design checks on your board. Items such as electrical model assignment, connector definition, power/ground net definition, discrete components, and electrical net definition are all in the Setup Wizard.

The scope of the checks can be defined with a specific list of design objects (e.g., power nets, capacitors) called an Object List. With a sophisticated filtering system, a specific object list with names, component values, part numbers, or any other property can be generated automatically.

In addition, the associated parameters for each rule can be edited based on technology and/or corporate guidelines.

Error Reports

Once you've run HyperLynx DRC, an error report is generated and you can select errors from the violation listing for viewing. In addition, Sharelist reports (containing the image, violation details, and coordinates) can be generated in HTML for broader team review.


Violation type: T-Fork Topology Violations (10)

N	Description	Net	Actual Value	Required Value	Severity	Status	Rank	Time Stamp	Rule name	Rule parameters	x, y coordinates	Screenshot
1	D0 length violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[6] [Clear/Zoomout]	2.1 in	1 in	Error	Unknown	1	3/3/2017 10:45:12 AM	Rules/SI/T-Fork Topology	MaxBranches='2' MaxDO='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.317 in, 3.945 in	att26713.jpg
2	#2 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[1] [Clear/Zoomout]	7.873 mil	0 mil	Error	Approved	1	3/3/2017 10:45:12 AM	Rules/SI/T-Fork Topology	MaxBranches='2' MaxDO='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.872 in, 4.179 in	att26717.jpg
3	#2 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[1] [Clear/Zoomout]	7.87 mil	0 mil	Error	ToBeFixed	1	3/3/2017 10:45:12 AM	Rules/SI/T-Fork Topology	MaxBranches='2' MaxDO='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.872 in, 4.012 in	att26718.jpg
4	#1 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[6] [Clear/Zoomout]	375.6 mil	0 mil	Error	Unknown	1	3/3/2017 10:45:13 AM	Rules/SI/T-Fork Topology	MaxBranches='2' MaxDO='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	9.16 in, 4.142 in	att26719.jpg

Spreadsheet - T-Fork Topology

	Description	Severity	Status	Rule name	Rank	Net	Rule parameters	Actual Value
1	D0 length violation	Error	Unknown	Rules/SI/T-Fork...	1	DDR2 ADDR[1]	MaxBranches='2'Ma...	1.998 in
2	#1 branch length matching viol...	Error	Approved	Rules/SI/T-Fork...	1	DDR2 ADDR[1]	MaxBranches='2'Ma...	174.9 mil
3	#2 branch length matching viol...	Error	Approved	Rules/SI/T-Fork...	1	DDR2 ADDR[1]	MaxBranches='2'Ma...	7.873 mil
4	#2 branch length matching viol...	Error	ToBeFixed	Rules/SI/T-Fork...	1	DDR2 ADDR[1]	MaxBranches='2'Ma...	0.00315 mil
5	#2 branch length matching viol...	Error	ToBeFixed	Rules/SI/T-Fork...	1	DDR2 ADDR[1]	MaxBranches='2'Ma...	5.75 mil
6	#2 branch length matching viol...	Error	ToBeFixed	Rules/SI/T-Fork...	1	DDR2 ADDR[1]	MaxBranches='2'Ma...	7.87 mil
7	#2 branch length matching viol...	Error	Unknown	Rules/SI/T-Fork...	1	DDR2 ADDR[1]	MaxBranches='2'Ma...	2.129 mil
8	#2 branch length matching viol...	Error	Unknown	Rules/SI/T-Fork...	1	DDR2 ADDR[1]	MaxBranches='2'Ma...	5.747 mil
9	D0 length violation	Error	Unknown	Rules/SI/T-Fork...	1	DDR2 ADDR[6]	MaxBranches='2'Ma...	2.1 in
10	#1 branch length matching viol...	Error	Unknown	Rules/SI/T-Fork...	1	DDR2 ADDR[6]	MaxBranches='2'Ma...	375.6 mil
11	#2 branch length matching viol...	Error	Unknown	Rules/SI/T-Fork...	1	DDR2 ADDR[6]	MaxBranches='2'Ma...	18.25 mil
12	#2 branch length matching viol...	Error	Unknown	Rules/SI/T-Fork...	1	DDR2 ADDR[6]	MaxBranches='2'Ma...	43.12 mil

Scalable Solutions

Design Issue	Rule Type	Rule	Free	Gold
SI	classic	Impedance	x	x
	classic	Edge rate		x
	classic	Guard trace		x
	classic	Long nets		x
	classic	Long stub		x
	classic	Many vias		x
	classic	Termination		x
	classic	Crosstalk coupling		x
	classic	Edge rate to period		x
	classic	Topology: Star		x
	classic	Via stub length		x
	DDR	Topology: T-fork	x	x
	DDR	Topology: Fly-by		x
	Diff pair	Differential impedance	x	x
	Diff pair	Differential pairs	x	x
	Diff pair	Diff-pair phase matching	x	x
PI	AC	Decap placement	x	x
	AC	Decap order		x
	DC	Power/Ground width		x
EMI	EMI	Metal island	x	x
	EMI	Net crossing gaps	x	x
	EMI	Signal supply		x
		number of rules:	8	22

For additional rules, subscribe to the low-cost HyperLynx DRC Gold Edition. The Gold Edition contains 14 additional SI, PI, and EMI/EMC rules, including crosstalk and stub checks for conventional SI checks, a fly-by topology check for DDR3/4, and a PI order check of decoupling capacitors.

Supported PCB layout systems and formats include:

- Mentor Graphics PADS®, Xpedition®, and Board Station®
- Cadence Allegro®, SPECCTRA®, and OrCAD®
- Zuken CADSTAR®, Visula®, CR-3000/5000/8000 PWS, and Board Designer
- Altium® Designer
- ODB++
- IPC-2581

For more information, call or visit:
www.mentor.com/pcb/hyperlynx/drc-free-edition

For the latest product information, call us or visit: www.mentor.com/hyperlynx

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

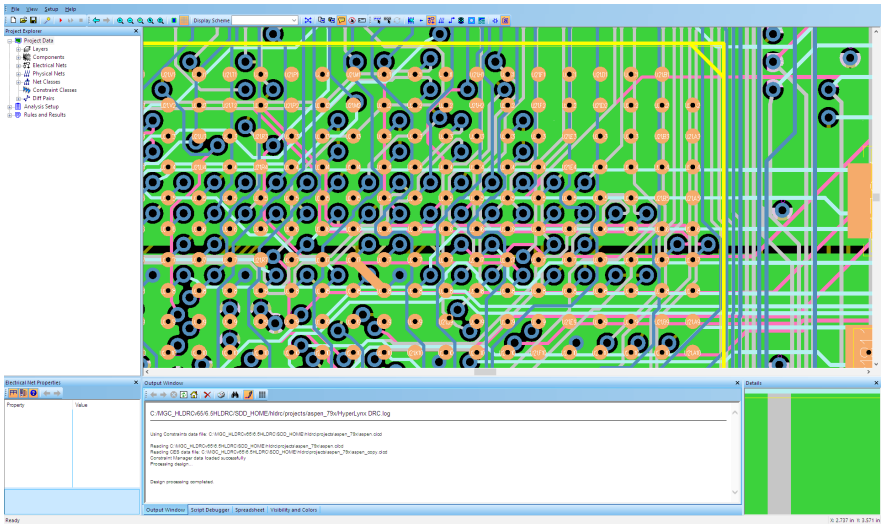
Mentor® A Siemens Business

MGC 06-17 1034680-w

HyperLynx DRC

Standard and Developer Editions

DATASHEET



Perform design rule checks on boards for electromagnetic interference and signal integrity issues with HyperLynx DRC.

Overview

HyperLynx® DRC is a powerful, fast, electrical design rule checking tool that automates the verification process and helps you perform design inspection iteratively. Use it to run complex checks for problems that are not easily simulated, such as rules for traces crossing splits, vertical reference plane change, and EMI/EMC. With HyperLynx DRC, you can go far beyond the error-prone, limited-scope DRCs built into layout tools.

The built-in DRCs can be parameterized by PCB designers and hardware engineers alike, as per technology and/or corporate routing or electrical guidelines. Its intuitive Project Setup Wizard makes design setup, rule running, and design analysis easy, irrespective of experience levels. With support for layout data from Mentor and non-Mentor printed circuit board (PCB) design flows, along with ODB++ and IPC-2581 standards, HyperLynx DRC fits seamlessly into your existing PCB process.

Use the script-writing and debugging environment of the HyperLynx DRC Developer Edition to write and execute custom rules to increase coverage of design verification coverage.

FEATURES AND BENEFITS

- 46 (HyperLynx DRC Standard) or 63 (HyperLynx DRC Developer) comprehensive SI, PI, EMI/EMC, safety, and analog checks
- Can be run directly from within Xpedition®
- Also supports layout data from PADS® and non-Mentor PCB flows
- Rule parameters can be edited based on technology or on corporate or IC vendor guidelines
- Advanced geometric and topological engines for efficient design rule checking
- Easy design setup and navigation
- Cross-probe to location of design violation from Sharelist (HTML format) error report
- Write and execute custom rules with HyperLynx DRC Developer
- Custom rule authoring supports JavaScript and VBScript and rule debugger (HyperLynx DRC Developer)

What's Included

The HyperLynx DRC Standard Edition lets you quickly and easily pinpoint trouble spots in your design that can cause potential signal integrity (SI), power integrity (PI), and electromagnetic interference and compliance (EMI/EMC) issues. Among the 46 built-in Design Rule Checks (DRCs) are ten rules for DDR compliance, ten rules for EMC compliance, and rules for relative delay and length matching and closed trace/return loop.

The HyperLynx DRC Developer Edition increases the scope of design verification with 17 additional DRCs. These include six safety rules for clearance, creepage, and regulation, three rules for analog compliance, and additional rules for general SI, such as differential pair symmetry and acute angle. In total, the Developer Edition supports 63 DRCs.

Built-in engines for geometric calculation, path finding, and net topology extraction, along with a 2D field solver, provide quick and accurate results without the need to prepare device models. With the HyperLynx DRC Developer Edition, JavaScript or VBScript can be used to access database objects using automation object models and then write and execute custom rules.

Easy Setup and Navigation

HyperLynx DRC is designed for quick and easy access to design data. A built-in Project Setup Wizard walks you through the steps for running design checks on your board. Items such as electrical model assignment, connector definition, power/ground net definition, discrete components, and electrical net definition are all in the Project Setup Wizard.

The scope of the checks can be defined with a specific list of design objects (e.g., power nets, capacitors) called an Object List. With a sophisticated filtering system, a specific object list with names, component values, part numbers, or any other property can be generated automatically.

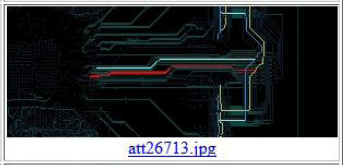
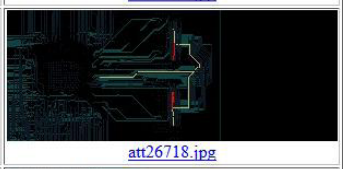
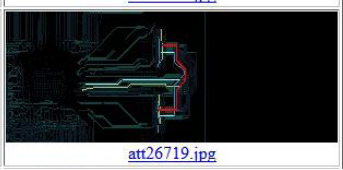
In addition, the associated parameters for each rule can be edited based on technology and/or corporate guidelines.

Error Reports

Once you've run HyperLynx DRC, an error report such as this list of t-fork topology violations is generated from where you can cross-probe to the location of the design violation. In addition, Sharelist reports (containing the image, violation details, and coordinates) can be generated in HTML for broader team review.

Rules			HyperLynx DRC	
			Standard Edition	Developer Edition
SI	classic	Impedance	◆	◆
	classic	Edge rate	◆	◆
	classic	Guard trace	◆	◆
	classic	Long nets	◆	◆
	classic	Long stub	◆	◆
	classic	Many vias	◆	◆
	classic	Termination	◆	◆
	classic	Crosstalk coupling	◆	◆
	classic	Edge rate to period	◆	◆
	classic	Topology -Star	◆	◆
	classic	Via stub length	◆	◆
	classic	Via to via isolation		◆
	classic	Acute angle		◆
	classic	Breakout & trace integrity	◆	◆
	Setup	Setup - add pin package delay and length	◆	◆
	DDR	Topology -T fork	◆	◆
	DDR	Topology - Fly-by	◆	◆
	DDR	Delay and length matching	◆	◆
	DDR	Relative delay and length matching	◆	◆
	DDR	Clamshell topology -length	◆	◆
	DDR	Clamshell topology -impedance	◆	◆
	DDR	Clamshell topology -diff pair impedance	◆	◆
	DDR	Group-to-group spacing	◆	◆
	DDR	In-group spacing	◆	◆
	DDR	Trace shielding	◆	◆
	DDR	Routing layer and trace type		◆
	Diff pair	Differential impedance	◆	◆
	Diff pair	Diff pair	◆	◆
	Diff pair	Diff pair symmetry		◆
	Diff pair	Diff pair phase matching	◆	◆
	Diff pair	Diff pair pad parasitic capacitance		◆
	Diff pair	Diff pair spacing		◆
	Diff pair	AC coupling cap value	◆	◆
PI	AC	Decap placement	◆	◆
	AC	Decap coverage		◆
	AC	Decap order	◆	◆
	AC	Decap via locations		◆
	AC	PDN isolation	◆	◆
	AC	Grounding layer	◆	◆
	DC	Power/ground width	◆	◆
	DC	PDN via count		◆
EMC	EMI	Exposed length	◆	◆
	EMI	IO coupling	◆	◆
	EMI	Closed trace /return loop	◆	◆
	EMI	Edge shield	◆	◆
	EMI	ICs over split	◆	◆
	EMI	Metal island	◆	◆
	EMI	Net crossing gaps	◆	◆
	EMI	Signal supply	◆	◆
	EMI	Net near plane edge	◆	◆
	EMI	Vertical reference plane change	◆	◆
	EMI	Filter placement	◆	◆
	EMI	Shield can location		◆
	ESD	Trace proximity	◆	◆
Safety	Clearance	3D clearance		◆
	Clearance	3D voltage clearance		◆
	Creepage	Same-layer creepage distance	◆	◆
	Creepage	Multi-layer creepage distance	◆	◆
	Regulation	Same-layer creepage for safety		◆
	Regulation	Multi-layer creepage for safety		◆
Analog	Oscillator	Nets under a component		◆
	Coupling	Component isolation		◆
	Sensor	Sensor net isolation		◆
Total number of rules			46	63

Violation type: T-Fork Topology Violations (10)

N	Description	Net	Actual Value	Required Value	Severity	Status	Rank	Time Stamp	Rule name	Rule parameters	x, y coordinates	Screenshot
1	D0 length violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[6] [Clear/Zoomout]	2.1 in	1 in	Error	Unknown	1	3/3/2017 10:45:12 AM	Rules/SI /T-Fork Topology	MaxBranches='2' MaxD0='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.317 in, 3.945 in	 att26713.jpg
2	#2 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[1] [Clear/Zoomout]	7.873 mil	0 mil	Error	Approved	1	3/3/2017 10:45:12 AM	Rules/SI /T-Fork Topology	MaxBranches='2' MaxD0='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.872 in, 4.179 in	 att26717.jpg
3	#2 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[1] [Clear/Zoomout]	7.87 mil	0 mil	Error	ToBeFixed	1	3/3/2017 10:45:12 AM	Rules/SI /T-Fork Topology	MaxBranches='2' MaxD0='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.872 in, 4.012 in	 att26718.jpg
4	#1 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[6] [Clear/Zoomout]	375.6 mil	0 mil	Error	Unknown	1	3/3/2017 10:45:13 AM	Rules/SI /T-Fork Topology	MaxBranches='2' MaxD0='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	9.16 in, 4.142 in	 att26719.jpg

Scalable Solutions

HyperLynx DRC is scalable, offering a variety of configurations to meet your needs. Use the questions in the following table to determine which product is best for you.

Customer need/environment	Free	Gold	Standard	Developer
Number of built-in rules	8	22	46	63
Rule complexity	Entry-level	Basic	Mid-level	Advanced
Licensing type	Subscription	Subscription	Time-based / Perpetual	Time-based / Perpetual
Need to parameterize rules?	◆	◆	◆	◆
Need to share results with others?	◆	◆	◆	◆
Need to import data from ODB^{++} or 3rd party?	◆	◆	◆	◆
Working on Windows?	◆	◆	◆	◆
Working on Linux?			◆	◆
Need to open HLDPROJ files?			◆	◆
Need to cross-probe from results to board viewer?			◆	◆
Need the ability to open SRs?			◆	◆
Currenly own HyperLynx DRC custom rules?				◆
Need to write corporate/technology rules?				◆

Supported PCB layout systems and formats include:

- Mentor Graphics PADS®, Xpedition®, and Board Station®
- Cadence Allegro®, SPECCTRA®, and OrCAD®
- Zuken CADSTAR®, Visula®, CR-3000/5000/8000 PWS, and Board Designer
- Altium® Designer
- ODB++
- IPC-2581

For more information, call or visit:
https://www.mentor.com/pcb/hyperlynx/electrical-rule-check

For the latest product information, call us or visit: www.mentor.com/pcb

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

Mentor® A Siemens Business

MGC 08-18 1034760-w

HyperLynx DRC Gold Edition

DATASHEET

Overview

Boasting fourteen more electrical rules than the HyperLynx® DRC Free Edition, the Gold Edition provides comprehensive electrical rule checking that is both proven and low cost. With the HyperLynx DRC Gold Edition, you can verify complex design rules that are not easily simulated, such as crosstalk coupling, decoupling capacitor order, and termination.

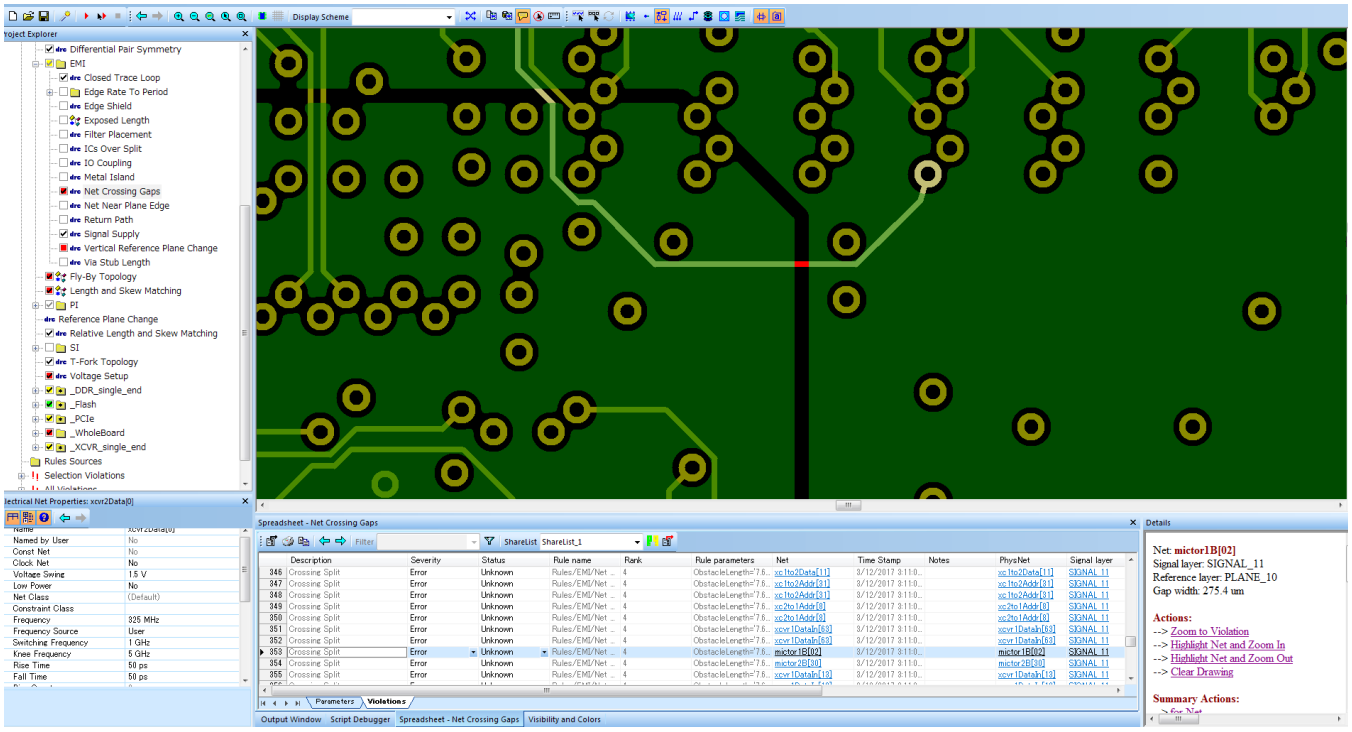
Both editions of HyperLynx DRC are fast and accurate, enabling you to perform design rule checking as often as desired during layout to catch problems early and eliminate problems before fabrication.

What's Included

HyperLynx DRC Gold contains 22 standard Design Rule Checks (DRCs) including 16 popular signal integrity rules and rules for basic power integrity and electromagnetic compliance. Built-in engines for geometric calculation, path finding, and net topology extraction, along with a 2D field solver, provide quick and accurate results without the need for preparing device models.

FEATURES AND BENEFITS:

- 22 comprehensive checks for SI, EMI/EMC, and PI
- Low-cost subscription pricing
- Rule parameters can be edited based on technology or corporate guidelines
- Advanced geometric engine for powerful and efficient design rule checking
- Easy setup and navigation
- Automatically generated HTML error report
- Support for all PCB layout formats
- Additional rules and custom rule development available in HyperLynx DRC Developer



Quickly and easily pinpoint trouble spots that can cause issues on your board with Signal Integrity, Power Integrity, and EMI/EMC. Automated net filtering suppresses false violations.

Design Issue	Rule Type	Rule	Free	Gold
SI	classic	Impedance	x	x
	classic	Edge rate		x
	classic	Guard trace		x
	classic	Long nets		x
	classic	Long stub		x
	classic	Many vias		x
	classic	Termination		x
	classic	Crosstalk coupling		x
	classic	Edge rate to period		x
	classic	Topology: Star		x
	classic	Via stub length		x
	DDR	Topology: T-fork	x	x
	DDR	Topology: Fly-by		x
	Diff pair	Differential impedance	x	x
	Diff pair	Differential pairs	x	x
	Diff pair	Diff-pair phase matching	x	x
PI	AC	Decap placement	x	x
	AC	Decap order		x
	DC	Power/Ground width		x
EMI	EMI	Metal island	x	x
	EMI	Net crossing gaps	x	x
	EMI	Signal supply		x
		number of rules:	8	22

Easy Setup and Navigation

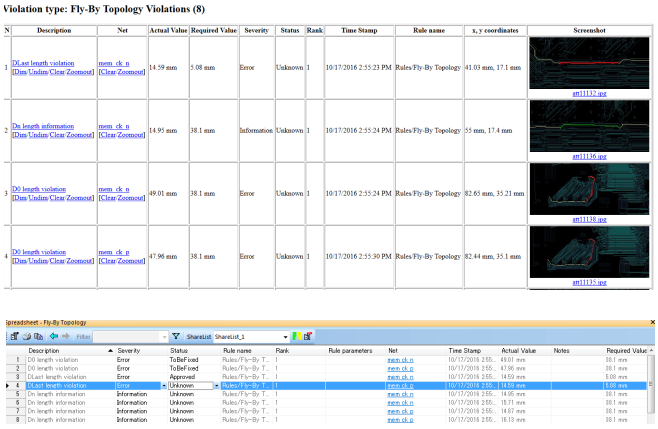
The HyperLynx DRC Gold Edition is designed for quick and easy access to design data. A built-in Setup Wizard walks you through the steps for running design checks on your board. Items such as electrical model assignment, connector definition, power/ground net definition, discrete components, and electrical net definition are all in the Setup Wizard.

The scope of the checks can be defined with a specific list of design objects (e.g., power nets, capacitors) called an Object List. With a sophisticated filtering system, a specific object list with names, component values, part numbers, or any other property can be generated automatically.

Each rule has pre-set parameters that can be customized and saved as different sets of design thresholds for various design requirements. For example, you can create specific rule sets for DDR2, DDR3, DDR4, PCIe, and USB2/3/3.1 just by modifying parameters.

Error Reports

Once you've run HyperLynx DRC, an error report is generated and you can select errors from the violation listing for viewing. In addition, Sharelist reports (containing the image, violation details, and coordinates) can be generated in HTML for broader team review.



Scalable Solutions

Mentor offers a number of electrical DRC configurations. The flagship product, HyperLynx DRC Developer, offers 63 rules including differential symmetry check for ultra-high speed SerDes and advanced EMC/EMI checking for vertical reference plane changes and nets near a plane edge. It also includes a built-in rule development environment in which you can write your own rules using VB Script or Java Script.

Supported PCB layout systems and formats include:

- Mentor Graphics PADS® Layout, Xpedition®, and Board Station®
- Cadence Allegro®, SPECCTRA®, and OrCAD®
- Zuken CADSTAR®, Visula®, CR-3000/5000/8000 PWS, and Board Designer
- Altium® Designer
- ODB++
- IPC-2581

For more information, call or visit:
www.mentor.com/pcb/hyperlynx/drc-free-edition

For the latest product information, call us or visit: www.mentor.com/hyperlynx

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

Mentor® A Siemens Business

MGC 09-18 1034690-w