USING FPGA I/O OPTIMIZATION TO DESIGN PCBS MORE COST EFFECTIVELY

ANDY WATTS, MENTOR GRAPHICS

WHITEPAPER

Mentor Graphics®

SYSTEM DESIGN

www.mentor.com

The power, flexibility and immediate availability of FPGA devices create compelling business drivers has generated a tsunami of FPGA adoption for the implementation of system PCB designs. Obviously, the time to market advantages and capacity/performance characteristics of FPGA devices have delivered on the promise for a viable alternative to more capital resource intensive custom IC/ASIC solutions as well as a successful consolidation vehicle for standard "off the shelf" components in system design creation.

The top-level FPGA perspective described above is the typical Engineering/Product Management perspective. While the typical FPGA-based project gains much economic and time-to-market benefit by using modern FPGAs, much unrealized benefit is left on the table. The simple truth is that the flexibility and power of the FPGA device is largely un-tapped as a source for system PCB optimization. The missing ingredient for full FPGA device flexibility exploitation is an analysis of the decision impact "domino chain" that begins with the PCB Signal to FPGA pin assignment and culminates with product profit margin.

This article demonstrates the causal relationship between PCB Signal to FPGA pin assignment and the product's profit margin. It also defines the opportunities to generate significant competitive advantages without significant time or cost penalties.

DETAILING IMPACTS TO PROFIT MARGIN

Most Engineering/Product managers would be stunned to learn that every PCB signal to FPGA pin assignment has a direct impact to their product profit margin. Analyzing the decision impact chain (Figure 1) shows that each time a PCB Signal is assigned to a FPGA pin both the FPGA and PCB design domains are impacted. While the impact of any single decision may be de minimis, the impact over several thousand such decisions can have a material impact on the cost, performance and reliability of the design. Within each design domain both the functional and physical aspects of the FPGA-PCB interface are available for alteration. By confining our analysis to the physical changes to the PCB interface, we may simplify the analysis without loss of focus on product profit margin.

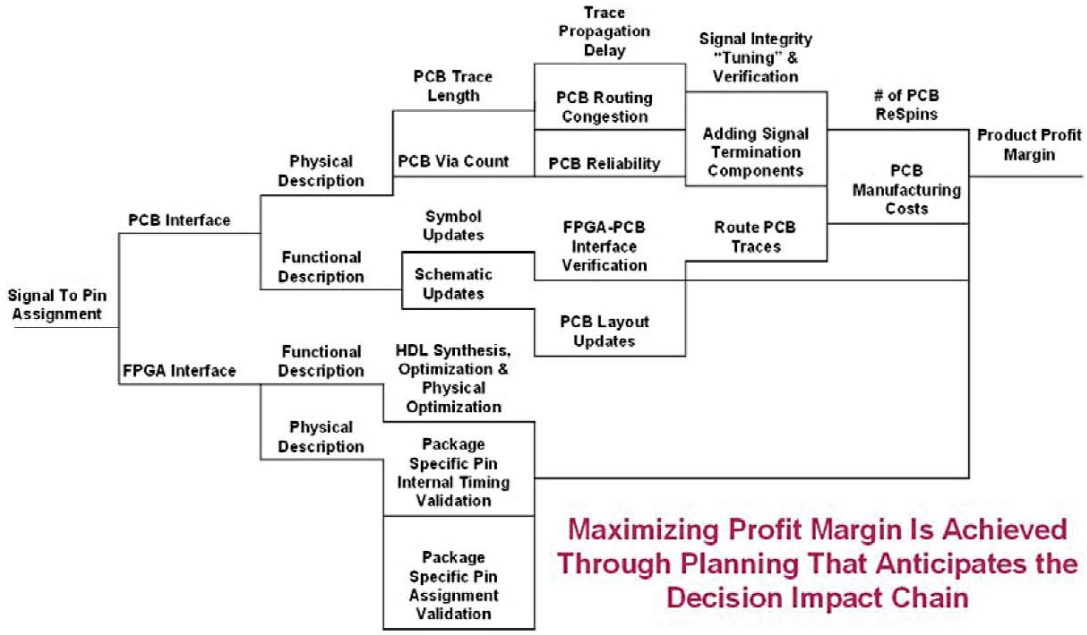

Figure 1: Anticipating decisions that will impact the design chain can improve profit margins.

Anytime a PCB signal is moved from one FPGA pin location to another FPGA pin location, both the PCB trace length, PCB via count and routing congestion are impacted. In the case of PCB trace length and routing congestion the impact is visually obvious, as clearly seen in Figure 2.

The two PCB signal to FPGA pin assignment options depicted in Figure 2 clearly demonstrate how the location of the physical connection point to the FPGA package impacts the length of PCB traces. In this example the PCB trace length was reduced by 50%, at the same time routing congestion and via count were reduced.

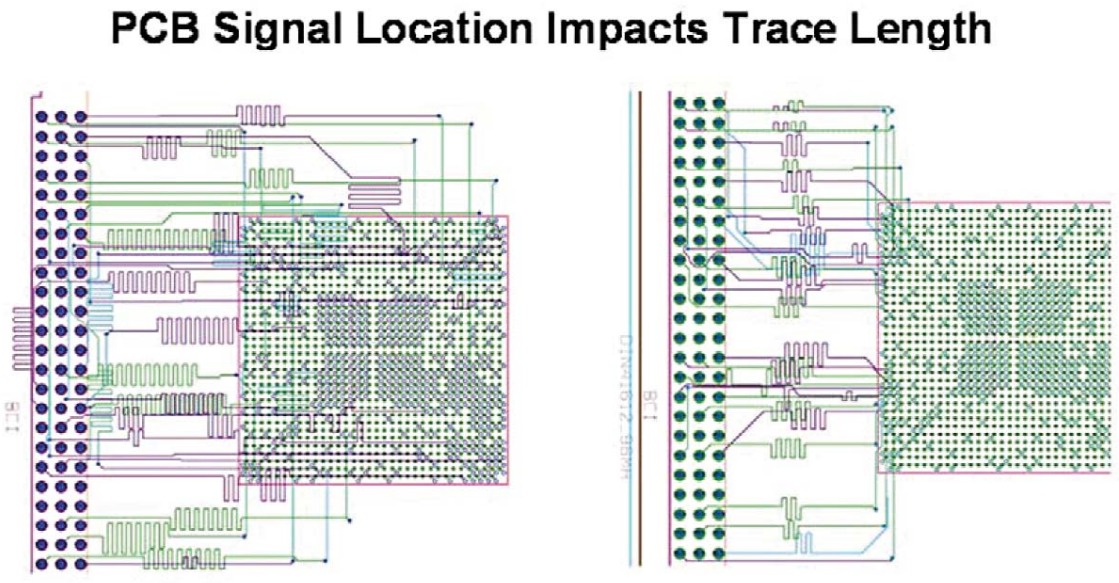

Figure 2: The location of the FPGA impacts the overall trace length, easily seen in these two views

Trace length impacts signal propagation delay across the trace. By reducing trace length by 50% propagation delay was reduced by 50% resulting in an increase of 100% for the maximum operating frequency of a signal operating across these traces.

Minimizing trace crossover through the flexibility of PCB signal to FPGA pin assignment increased the reliability of our PCB system design too, as PCB vias are susceptible to vibration and consequently are potential mechanical and electrical failure points. While the impact to routing congestion is visually obvious, attributing statistical characteristic to routing congestion requires a careful measurement of the surface area consumed by both signal assignment options. In our trivial example routing congestion was reduced by approximately 20%.

Clearly, PCB signal to FPGA pin assignment impacts:

- PCB trace length
- PCB propagation delay
- PCB reliability
- PCB routing congestion

ACCELERATING SYSTEM CONSTRAINT CONVERGENCE

How much time is spent in the design cycle "tuning" the PCB design to meet timing and signal integrity constraints? While "the shortest distance between two points is a straight line" is accurate it is also true that the shortest distance is achieved when the "two points" are moved as close to each other as possible. The magic of FPGA devices in system PCB designs is that one of the two points in an electrical connection is flexible.

Instead of spending excessive amounts of design time "tweaking and tuning" the PCB design to meet system constraints by altering component placement, component rotation, PCB layer stackup, PCB signal layer pairs, trace routing and possibly PCB manufacturing materials, the pragmatic approach is to leverage the FPGA's inherent flexibility. By minimizing the connection distance between the FPGA and the other components on the PCB system first the time spent "tweaking and tuning" may be reduced from 20%-50%.

ACCELERATING SYSTEM PHYSICAL DESIGN AND MINIMIZING MANUFACTURING COSTS

Likewise, a high quality FPGA-PCB interface design can reduce the amount of design cycle time spent routing traces on the PCB from 25% to 50%. One critical value delivered by FPGA flexibility to the system design is a reduction of routing congestion that creates additional signal layer pair surface area that may be used to route additional traces. When the routing congestion trend is applied to high pin density FPGA packages it is quite possible that a high quality FPGA-PCB interface will reduce the number of signal layer pairs required to implement complex systems. The resulting savings in manufacturing costs from a single signal layer pair reduction are consequential for moderate production volumes.

Leveraging the flexibility of FPGA devices to reduce routing congestion is a proven method for taking an "un-routable PCB" and transforming it into a "routable PCB" without adding to PCB manufacturing costs. The opportunity often overlooked is the time required to determine that the current PCB layer stackup does not provide the trace routing surface area necessary to complete the design…the amount of time before the declaration of an "un-routable PCB".

PROFIT MARGIN IS THE LAST DOMINO IN THE IMPACT DECISION CHAIN

The logical decision impact chain from FPGA-PCB interface design to product profit margin is a simple "domino cascade." The domin's fall whether or not the engineering community is consciously aware of their linkage. The simple truth is that many system design teams are unaware of the decision impact chain simply because it crosses design domain boundaries as well as creates clashes with historic and cultural design processes.

UNDERSTANDING THE BARRIERS TO PCB OPTIMIZATION

If the flexibility of FPGA devices may be used to optimize PCB designs why is this flexibility so infrequently leveraged by design teams?

- Design Complexity
- Risk Analysis and Aversion
- Design Team Organization and Silos
- Traditional Design Processes
- Historic Design Support Infrastructures
- Time to Market Constraints
- Availability Of Tools

DESIGN COMPLEXITY

In fundamental terms creating a legal FPGA interface definition is non-trivial. Consider the number of possible signal to pin interface designs:

- A two signal pin package has 2 possible interface designs
- A three signal pin package has 6 possible interface designs
- A four signal pin package has 24 possible interface designs
- A five signal pin package has 120 possible interface designs
- A small one hundred signal pin FPGA package has 9 x 10157 possible interface designs
- A common one thousand signal pin FPGA package has so many possible interface designs that Microsoft Excel is unable to calculate the value

The space of all possible FPGA interface designs contains both legal and illegal pin assignment definitions. The difference between a legal and illegal interface design is defined by the FPGA Vendor pin assignment rules on a device/package/pin specific basis.

The number of possible interface designs is only one dimension of the complexity. Each FPGA signal pin may be defined as one of N possible I/O Standards where "N" may be as great as 78, as shown in figure 3. The FPGA Vendor pin assignment rules are dynamic and evaluate pin type, I/O Standard setting and pin bank as primary variables.

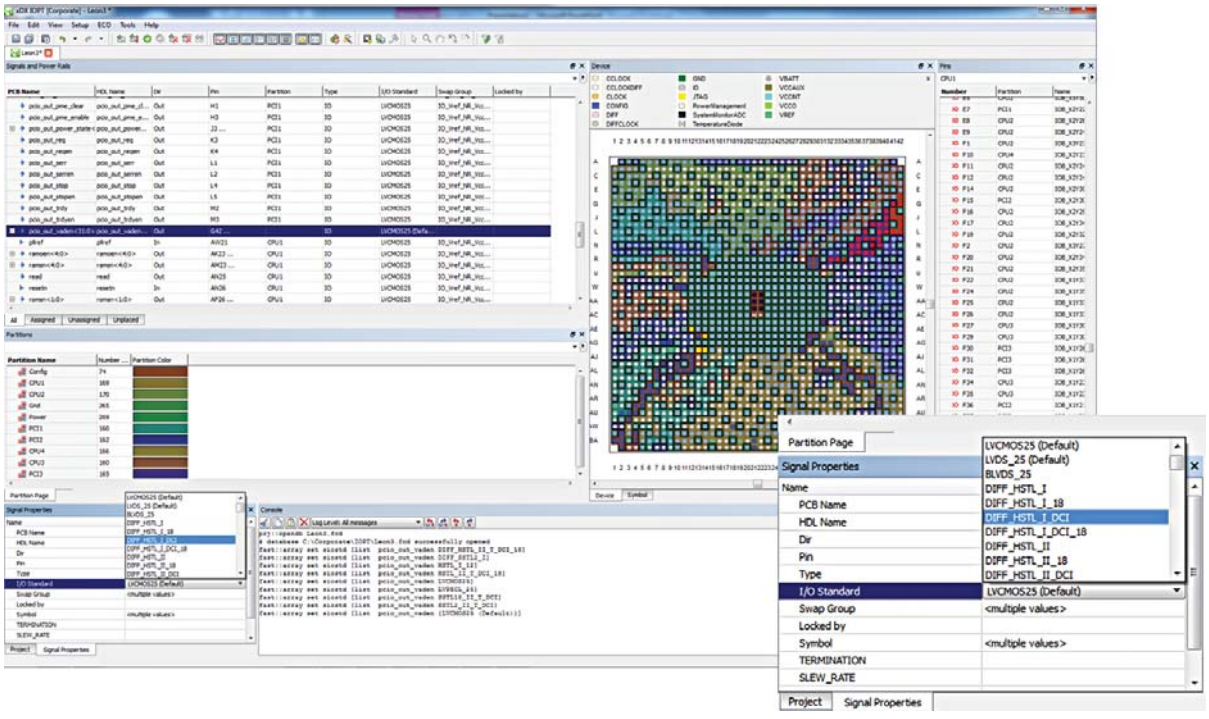

Figure 3: A given pin may have as many as 78 different I/O Standards which might apply. Xpedition's FPGA I/O optimizer maintains the standards and presents designers with possible standards for their choice.

A simple example: A 3.3V I/O standard may not co-exist with a 1.8V standard within the same pin bank (Power region). It is not until PCB signals are assigned to the FPGA pins and the FPGA pins are electrically configured to match the signal that "pin swap rules" are defined for the FPGA component.

The simple example illustrates a primary difference between FPGA devices and standard off the shelf components in terms of their interfaces but obfuscates the true complexity of FPGA interface design. Every FPGA device/package has complex and varying FPGA interface design rules. Multi-purpose pins abound on FPGA devices:

- Clock pins that could be used as I/O Signal Pins
- I/O Signal pins that could be used a local clock pins
- FPGA Configuration (boot) pins that could be used as I/O Signal Pins
- JTAG pins that could be used as I/O Signal Pins
- I/O pins with variable drive strength settings
- I/O pins with variable slew rate settings
- I/O Pins with variable termination topology settings
- I/O pins that could be a differential pair signal pin as long as the polarity is Positive
- I/O pins that could be a differential pair signal pin as long as the polarity is Negative
- Vref pins that could be used as I/O pins as long as the no I/O pins within the same pin bank demand a reference voltage

That's the short list. Typically, a few months are required for an engineer to gain the FPGA device/package expertise required to effectively create legal FPGA interface designs. This FPGA device/package expertise required is not common knowledge across the complete system design team creating natural bottlenecks in the design process.

RISK ANALYSIS AND AVERSION

The risk introduced through leveraging FPGA-PCB interface flexibility is simple: If a single error exists in the FPGA-PCB interface between FPGA and PCB design flow domains the resulting PCB will be non-operational. In worst case scenarios the FPGA-PCB interface error may cause catastrophic component damage (e.g. driving 20mA into a pin rated to accept 5mA). The costs associated with the interface errors greatly exceed any PCB manufacturing prototype costs; the real cost is to the design cycle time budget when weeks of expensive engineering time are consumed comparing PCB symbols and schematics to the FPGA design and vendor files to discover the exact error(s). This is a tedious and painful process that any experienced engineer will systematically avoid.

The natural and common design team reaction to the design complexity associated with FPGA – PCB interfaces and the need to maintain absolute synchronization of the Interface across design domain boundaries is to lock the FPGA-PCB interface design early in the design process.

If we were discussing a situation where we had a couple dozen of pins that comprised the FPGA-PCB interface the interface error risk and signal complexity assignment would not be compelling drivers. However, we are dealing with devices that have hundreds-to-thousands of signal pins. When the atomic pin complexity is multiplied by the number of signal pins on the FPGA device and then factored by FPGA pin co-habitation rules and then analyzed to determine the dimensions of the decision impact chain there are billions of possible impacts to your product profit margin to consider.

DESIGN TEAM ORGANIZATION AND SILOS

To achieve PCB optimization the FPGA design team, the PCB Functional design team and the PCB physical design teams must all be in harmony. Many design organizations have evolved from the "chip vs. board" structure to a "system" team comprising both FPGA and PCB functional engineers. At the same time primary business drivers have generated a chasm between functional design and physical design through outsourcing and "design anywhere, build anywhere" initiatives. At some point in the product design process the electronic design is "thrown over the wall" from one team to another creating organizational silos. Transcending the existing silos to achieve PCB optimization requires focused management effort to promote effective communication while minimizing design re-spin risk.

TRADITIONAL DESIGN PROCESSES

The dominant process for creating system PCB functional designs remains schematic based. The historic advantage of schematic design process is the accurate communication of design intent through a symbolic representation. Schematic based design methods have intrinsic costs and risks:

- Symbols for all components used in the design must be created and verified
  - Symbol interface errors result in non-operational PCBs
- Creating schematics and connecting the components is labor intensive and time consuming
  - Schematic errors result in non-operational PCBs

Creating a single symbol for a 500+ pin FPGA device is labor intensive, time consuming, error prone and could result in the symbol not physically fitting on a schematic sheet. To overcome the size issue design teams will often create multiple (fractured) symbols for a single FPGA device slightly increasing the labor, time and validation investment. In order to be able to re-use the investment in FPGA symbol creation generic fractured symbols are often created based on FPGA pin bank.

The caveat to generic FPGA fractured symbols is that it is technically impossible to include FPGA pinswap data as the pin-swaps are design specific. Additionally, the value of the schematic to clearly convey design intent is obfuscated while maintaining the costs of the schematic design process.

At this level of detail there is no mystery as to why design teams are reluctant to leverage the flexibility of FPGA interface design to optimize their PCB: The costs and risks associated with the symbol and schematic creation, maintenance and validation process preclude "flexibility".

HISTORIC DESIGN SUPPORT INFRASTRUCTURE

Many electronic design corporations have instituted PCB corporate libraries and processes/policies to minimize the risk associated with errors in "off the shelf" component interfaces. Off the shelf components historically have a common attribute: The interface to the component never changes. It is worthwhile to invest in creating and verifying a high quality interface for standard "off the shelf" components since the work is done once and then leveraged in designs incorporating that component.

The same logic has been erroneously applied to FPGA devices in an attempt to minimize risk associated with the incorporation of FPGA devices into complex system designs. A simple truth is overlooked: FPGA interfaces are design specific and change with every design. The artifact of applying historic risk mitigation logic to FPGA components results in a condition where FPGA pin swaps are not allowed in the standard design process. While a good argument exists that the PCB physical designer does not typically posses the FPGA interface design expertise to create a legal pin swap the net result is a significant loss of design flexibility that could be leveraged to optimize the PCB design.

TIME TO MARKET CONSTRAINTS

Time to market is often a fundamental driver in the selection of FPGA devices for inclusion in system PCB designs. With the design development window under constant pressure to shrink a key aspect of meeting time to market constraints is design risk mitigation.

As demonstrated by other barriers to PCB optimization leveraging the flexibility of FPGA devices for PCB optimization is key source of increasing design schedule risk. It is true that leveraging the flexibility of FPGA interface design has repeatedly proven to substantially reduce time to market. It is also true that is statement is only valid when advanced design technologies are deployed to systematically address every PCB optimization barrier concurrently.

AVAILABILITY OF TOOLS

Every FPGA Vendor supplies tools that will automatically create a device/package specific legal signal to pin assignment. However, none of these solutions consider anything but a single FPGA in the creation of the interface. The PCB physical connectivity is never considered by the FPGA Vendor tools. To be fair, it would be a resource/expertise investment misalignment to expect the FPGA Vendors to supply tools that consider the PCB layout.

Consider using multiple FPGA devices on the same PCB with each FPGA package containing 1500 pins. The idea that the design optimization space may be adequately evaluated to achieve PCB optimization manually exceeds any reasonable expectation once the design complexity is understood. This is clearly a problem space where computer based optimization is the only practical alternative. Mentor Graphics is the only top-tier EDA supplier with a track record demonstrating sustained investment to produce products focused on achieving PCB optimization through FPGA interface design flexibility.

BARRIER SUMMARY

It is the combination of risk assessment, historic and cultural processes and policies, required expertise, as well as the elemental interface complexity (the number of possible interface designs) that create the natural motivation to implement the Draconian practice of locking down the FPGA-PCB interface early in the design process. It is the unjust harshness of locking the FPGA-PCB interface early that precludes PCB optimization and puts your product profit margin outside the normal engineering design process.

THE POTENTIAL EXISTS

Capitalizing on the emergence of FPGA adoption and leveraging the power of FPGA interface flexibility has allowed early adopters of PCB optimization technology to experience fantastic results:

- Eliminating a minimum of one man-week per 500 FPGA pins on the system PCB design.
- Reducing trace length by 25% to 50% and enjoying a corresponding performance increase
- Eliminating up to 150 PCB vias for every 500 FPGA pins
- Reductions in interface design times as much as 60%
- Transforming un-routable PCBs into routable PCB using the same PCB layer stackup
- Total design cycle reduction by as much as 50%

In a competitive landscape where fighting for a nickel of PCB manufacturing cost advantage and a day of time to market acceleration could define the difference between windfall profits and a “boat anchor” there are not many opportunities to realize a 50% design time to market advantage.

THE POWER OF THE TSUNAMI

Cleary, taking advantage of the flexibility of FPGA devices to optimize PCB design for product profit margin is a critical evolution of standard system PCB design processes. The truth is that this level of PCB optimization represents the first plateau in PCB optimization opportunities.

What about those system PCB designs that use more than one FPGA device? What if the system design complexity demands 3, 4, 10, 20 FPGA devices? Without basic PCB optimization these designs are doomed to encounter the "un-routable PCB" engineering euphemism. Experience has demonstrated that when the system design calls for one or two high-pin-density FPGA devices, your design team has the expertise, experience, dedication and work ethic to "get the job done". Chances are they never had the opportunity to consider profit margin optimization but they met the schedule and the product works. Once you have more than 4 of these large FPGA devices on the PCB your engineering team will "hit the wall" where their dedication will be betrayed by either skyrocketing PCB manufacturing costs as the signal layer pairs increase or the dreaded "un-routable PCB".

Customers entrenched in their corporate infrastructure, processes and policies often confront PCB optimization for the first time when they attempt more complex system PCB designs containing multiple FPGA devices. A common reaction is an attempt to either reduce the number of FPGA devices by finding larger devices and/or re-architecting the system design to reduce complexity...anything but confronting the barriers and opportunities associated with PCB optimization.

Applying PCB optimization technologies simultaneously across multiple-FPGA system designs represents the next plateau of PCB optimization. A key requirement for multi-FPGA optimization is the ability to optimize across multiple FPGA devices that may span multiple FPGA Vendors. The ability to bring together FPGA device/package specific intelligence spanning multiple FPGA Vendors for a simultaneous PCB optimization is a requirement only an EDA PCB Supplier has an opportunity to meet.

Are you aware that FPGA pin electrical flexibility could be used to eliminate additional components from your PCB? Through modifications of pin electrical characteristics discrete signal conditioning components may be eliminated from the system PCB design. Most design teams are trapped in the "time-to-market" crunch and never have the opportunity to research this level of PCB optimization let alone develop the necessary technical skills to wield this advanced FPGA power and flexibility.

No attempt should be made to underestimate the expertise required to achieve discrete component elimination through the manipulation of FPGA pin electrical characteristics:

- Pin electrical characteristic changes have mirror impacts both "inside the FPGA package" and "outside the package" on the PCB
- PCB signal integrity and timing analysis tools and usage "expertise" must be "at the ready" to evaluate each and every proposed electrical characteristic change
- As soon as utilization of on-chip FPGA termination is considered an appropriate "paranoia" (not an exaggeration) must be developed focused on Simultaneous Switching Output Noise

At the same time, underestimating the competitive advantages obtainable through the minimization of PCB component costs and the corresponding positive impact to product profit margin would open the door to your competition. When combined with newer High Density Interconnect (HDI) PCB manufacturing processes significant PCB manufacturing cost savings are possible and sufficient justification for some system PCB design teams to make substantial investments to reach the next PCB optimization plateau.

The doorway to PCB optimization has been opened but the final destination has no road markers. The power and flexibility of FPGA devices continues to evolve as well as the expertise and experience of using that flexibility and power to optimize PCB designs. The survival question to ask yourself is: Are you on the PCB optimization path?

THE EDA TOOLS EXIST TODAY

With over a decade of sustained investment after early identification of the opportunity manifest in FPGA devices to optimize PCB designs, Mentor Graphics, in partnership with FPGA vendors, has developed the I/O optimization family of products that provide easy-to-achieve PCB optimization while simultaneously eliminating any FPGA-PCB interface error risk and scaling to provide simultaneous multi-FPGA optimization, as illustrated in figure 4. The combination of technology leadership and strong partner-customers supported the development and validation of PCB optimization as a key competitive advantage for system PCB design teams.

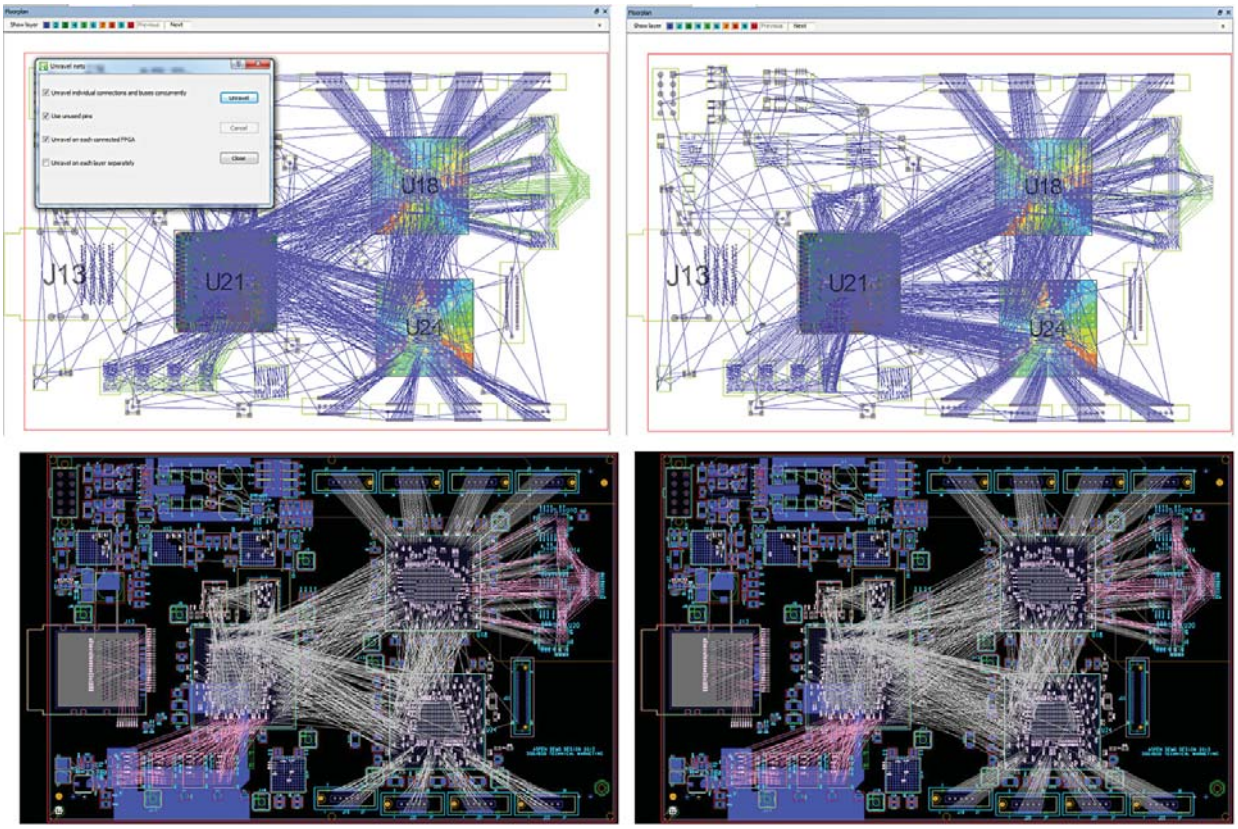

Figure 4: I/O optimization using Xpedition FPGA I/O optimizer. On the left, before optimization and on the right after.

For the latest product information, call us or visit: www.mentor.com

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

MF 6-15 TECH7740-w