STMICROELECTRONICS QUICKLY BRINGS AUTOMOTIVE IMAGE SIGNAL PROCESSING TO MARKET WITH HIGH-LEVEL SYNTHESIS

MARC SCHMITZ, IMAGING PRODUCT DIGITAL DESIGN MANAGER,
STMICROELECTRONICS

life.augmented

Mentor®
A Siemens Business

WHITEPAPER

HIGH-LEVEL SYNTHESIS

www.mentor.com

INTRODUCTION

The STMicroelectronics® Imaging division is responsible for delivering innovative imaging technology and products to the consumer, industrial, security, and automotive markets. The team has crafted a unique High-Level Synthesis (HLS) flow, enabled by templates, that brings these products quickly to market. For the automotive market, this flow complies with the ISO 26262 standard to ensure reliability. This paper covers how the team uses their HLS flow to design and verify an image signal processing (ISP) device, getting it to market as fast as possible.

The ISP is a combination of hardware and software that processes image sensor data. The ISP can be very complex, so the team assembles the design using reusable IP modules. Figure 1 shows a sample ISP block diagram.

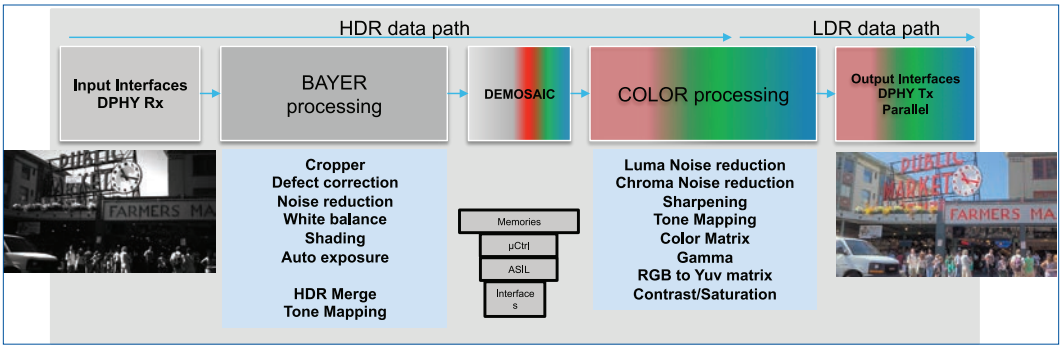

Figure 1: Complex, high-quality ISP for automotive applications

The ISP in Figure 1 shows the main ISP functions and illustrates the many processing algorithms that are necessary along the data path.

UNDERSTANDING THE HLS TOOL HISTORY

The Imaging division started employing an HLS design flow in 2007 for multimedia IP (encoders, decoders, displays, and ISP functionality) using a tool from a Mentor competitor. When that tool was discontinued in 2015, the team evaluated several HLS tools from various vendors by applying several ISP designs as test cases and monitoring the area and power results of the generated RTL. Based on this evaluation, the team selected the Catapult® High-Level Synthesis Platform because of its superior results.

The Catapult HLS Platform empowers designers to use industry-standard ANSI C++ and SystemC to describe functional intent, moving up to a more productive abstraction level. From these high-level descriptions, Catapult generates production-quality RTL. By speeding time to RTL and by automating the generation of bug free RTL, Catapult significantly reduces the time to verified RTL. Catapult's advanced power optimizations automatically provide significant reductions in dynamic power consumption. The highly-interactive workflow provides full visibility and control of the synthesis process, enabling designers to rapidly converge upon the best implementation for power, performance, and area (Figure 2).

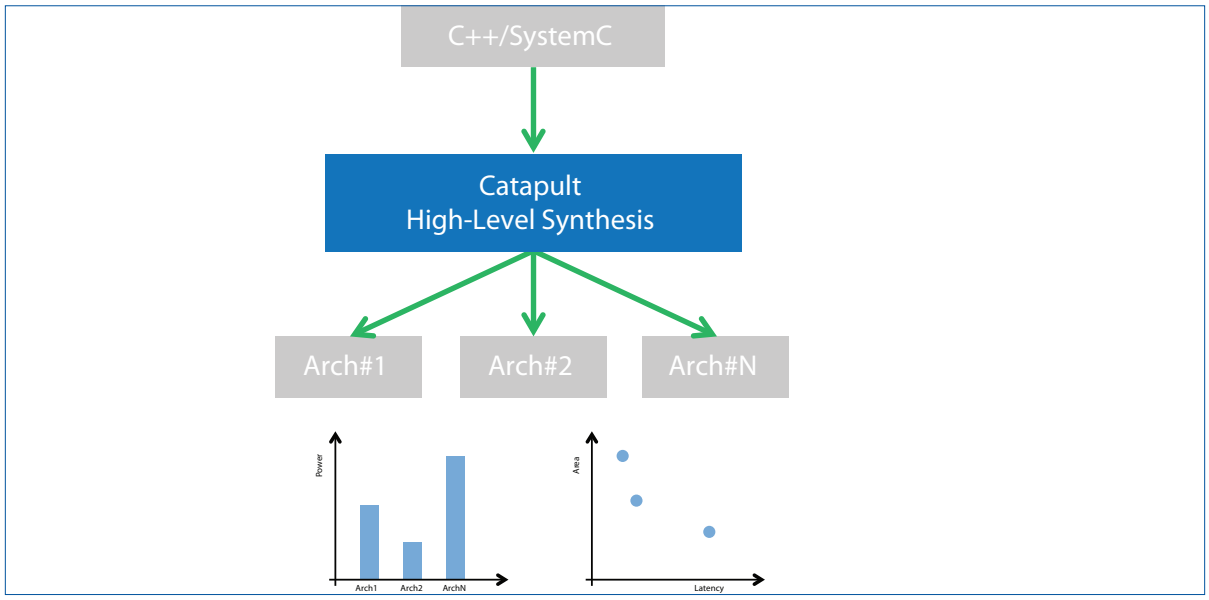

Figure 2: Rapidly explore architectures to find the best power and area

CREATING IMAGING IP TEMPLATES

The team realized that an ISP is a cascade of filters and that these filters have similar structures and interfaces. Their idea was to develop a library of parameterized filters using C++ templates and then reuse them for each ISP design. The benefits of this approach include:

- Design efficiency: it is faster to build up the ISP by reusing proven templates.
- Updates: it is easy to propagate updates to each IP block and algorithm changes can be integrated in a single day.
- Focus: the designers can spend their time developing value-added algorithms and not worry about the common structures.
- Resources: the team can develop more IP blocks for a project without adding extra staff members.

Each parameterized template is a C++ class (Figure 3) that establishes:

- Memory management
- Protocol bridge
- Kernel of pixel management
- Connection to the testbench

The designer overrides the *filterFunction* to provide the algorithm code and then connects it to the filters by overriding the execute function.

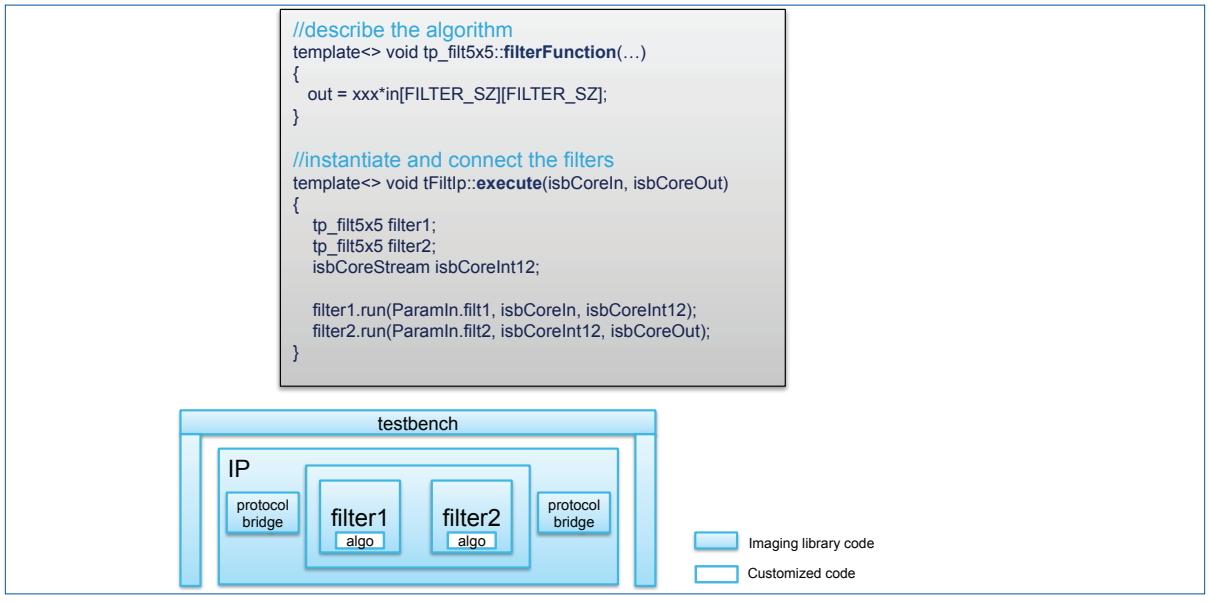

Figure 3: Designers focus on algorithms, not infrastructure

Using this template process, the team has created more than 50 designs over the last two years, ranging in size from 10K gates to 2 million gates.

VERIFYING THE DESIGN

The team uses UVM testbenches that specify sequences that provide pseudo-random verification and collect code and functional coverage metrics. The team uses the same testbenches, without modification, to verify the C++ and the generated RTL design. Each testbench (Figure 4) establishes the same set of criteria for each project, which reduces development time by automating the verification environment setup. This criteria includes standardized:

- Input and output interfaces for data
- Register configuration interfaces
- High-level control (enabling and resetting the design)
- Input and output data format

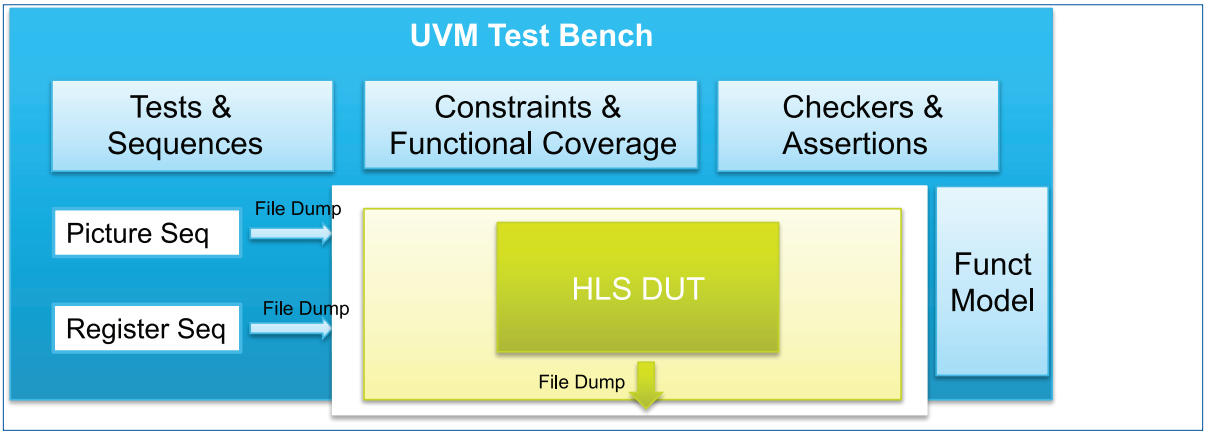

Figure 4: Common UVM testbench to simulate either the C++ (shown) or RTL device under test

The common UVM testbench elements include the tests and sequences that exercise the device under test (DUT), the constraints and functional coverage statements, and many checkers and assertions. Picture and register sequences exercise the DUT inputs. The team uses the functional model for bit-true comparison against the DUT.

The team ensures the best quality of the design by using the same verification methodology for each project (Figure 5).

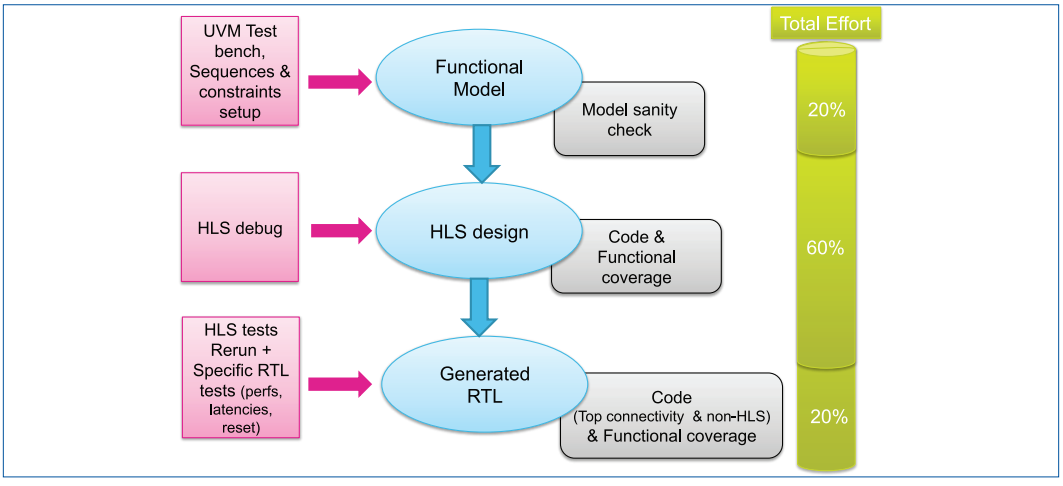

Figure 5: The verification flow

The high-level steps of the HLS verification flow include:

1. The designers create a functional model and the verifiers build the UVM testbench with the necessary sequences and constraints. The simulation at this stage provides a "sanity" check for the overall environment and can identify issues.
2. The HLS debug step consumes the most time within a project. Here, the sequences are run to debug issues and to collect code and functional coverage metrics.
3. Using the same UVM testbench, the team simulates the RTL that Catapult HLS generates. Here, the team adds some specific RTL tests that target functionality that is not modeled in the C++ design, such as latency between inputs and outputs and reset behavior. This step also simulates any RTL that is not generated in the HLS flow (if any). The team collects code and functional coverage metrics from the top level of the design at this point.

MEETING THE ISO 26262 STANDARD

Many of the ISP products target the automotive market, which means the team must follow the ISO 26262 standard. ISO 26262 is a standard for functional safety of electrical & electronic components in road vehicles weighing up to 3500 kg. The team ensures that the HLS flow and design robustness meets the standard (Figure 6).

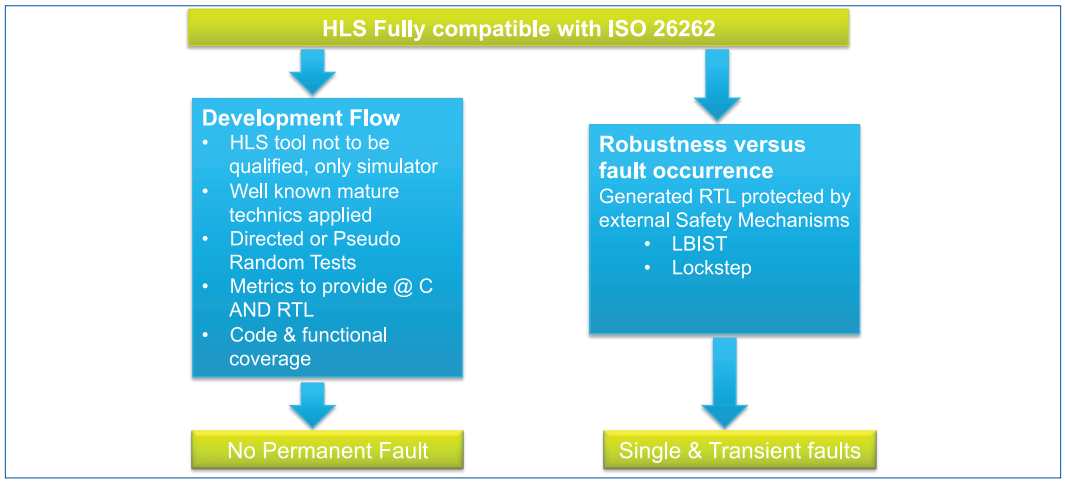

Figure 6: ISO 26262 is compatible with the HLS flow

A key requirement of the standard is to ensure that the device does not have a permanent fault (a bug in the design). This means that the team must ensure that the development flow is "safe." Applying mature techniques, performing an array of tests, and collecting metric reports satisfies the standard. The team does not qualify the Catapult HLS Platform for ISO 26262. Instead, they qualify the simulator that runs the tests. While the team does not require qualification of the Catapult HLS Platform within their flow, the Mentor Safe program does provide ISO 26262 qualification and documentation for the tool.

The next major requirement is to ensure that the design can handle and recover from single or transient faults. The team confirms robustness by surrounding the ISP with external safety mechanisms such as LBIST and lockstep.

REAPING THE BENEFITS OF THE HLS FLOW

The major benefit of the HLS flow with templates is that development time and cost is heavily reduced with no compromise in results and design quality (Table 1). Using the flow, the team creates the design 3X faster than hand-coding and a single designer can perform verification, typically eliminating the need for a separate verifier resource.

CODE	DESIGNER	VERIFIER	TOTAL
HAND-WRITTEN RTL	12 Weeks	12 Weeks	24 Weeks
GENERATED RTL FROM HLS	6 Weeks	8 Weeks	14 Weeks
USING TEMPLATES IN HLS FLOW	8 Weeks	0 Weeks	8 Weeks

Table 1: Average time spent for an ISP design project by one designer and one verifier

Development cost is further reduced because:

- Verification using C++ to collect key coverage metrics means that the team can run thousands of tests in minutes versus hours that it would take for RTL.
- Significantly fewer lines of C++ code versus RTL means that the cost of maintenance is dramatically less.
- A change in the specification late in the design flow can easily be accommodated without disruption to schedule.
- 10 designers were trained on the HLS flow in only a few days, meaning that the team could be productive quickly.

In addition, development time and cost is lower in the HLS flow due to Catapult HLS Platform features that automate the design implementation:

- Automatic pipelining: a simple change of directives drives the level of pipelining while retaining the same C++ code. Considerable recoding and debugging is required if pipelining by hand.
- Automatic hardware sharing: for example, reusing a multiplier for several operations of the same iteration at different states of a pipeline, is very difficult to do by hand.
- Automatic functional clock gating: saves considerable time versus hand coding and can automatically reduce power by 10%.

The team found that quality of results of the generated RTL from the tool was excellent, especially for complex designs.

To learn more about the Catapult HLS solution, click here.

ABOUT MARC SCHMITZ

Marc Schmitz manages the digital design and verification teams in the STMicroelectronics Imaging division, which is focused on image sensors and Time-Of-Fight products for consumer and automotive markets. After a Dipl.-Ing. Degree from Phelma School in Grenoble, Marc started at STMicroelectronics in 2004 as a verification engineer and has worked on many projects, such as microcontrollers and the Multimedia Engine for Application Processor. His technical expertise encompasses verification and design flows including high-level synthesis, which was introduced in 2007 to the design process.

This whitepaper was derived from a Verification Academy presentation delivered by Marc Schmitz in June 2017 at DAC.

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

MGC 10-17 TECH16140-w