ELIMINATE SCHEMATIC DESIGN ERRORS WITH AUTOMATED VERIFICATION

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THE CHALLENGE – ELIMINATE SCHEMATIC DESIGN ERRORS

The schematic is the controlling document for every Printed Circuit Board (PCB) design. It captures the design intent and drives all downstream processes including simulation, analysis, layout, fabrication, and assembly. As such, it is critical that the schematic accurately reflects the product's electronic requirements and specifications.

Historically, the all-important task of verifying that the schematic is properly conveying design intent has been a manual process conducted by one or more hardware engineers. This verification is usually performed one sheet or one block at a time, with some automation used to assist in the process such as exporting the bill-of-materials and/or the netlist to text files or spreadsheets.

Schematic verification is an accepted part of the hardware engineer's responsibility just as PCB layout verification is an accepted part of the PCB designer's responsibility. However, with today's circuit designs becoming more and more complex, time-consuming manual schematic verification is no longer an option. Manual verification of a complex circuit introduces significant risk by not identifying schematic design errors that are, in turn, passed to the downstream processes and ultimately to the fabricated board. This results in costly respins and increased time to market.

Today's schematics are just too complicated to verify reliably by hand. 65% of the companies surveyed in a recent study conducted by the Aberdeen Group cited increasing product complexity as their top PCB design challenge (Figure 1).

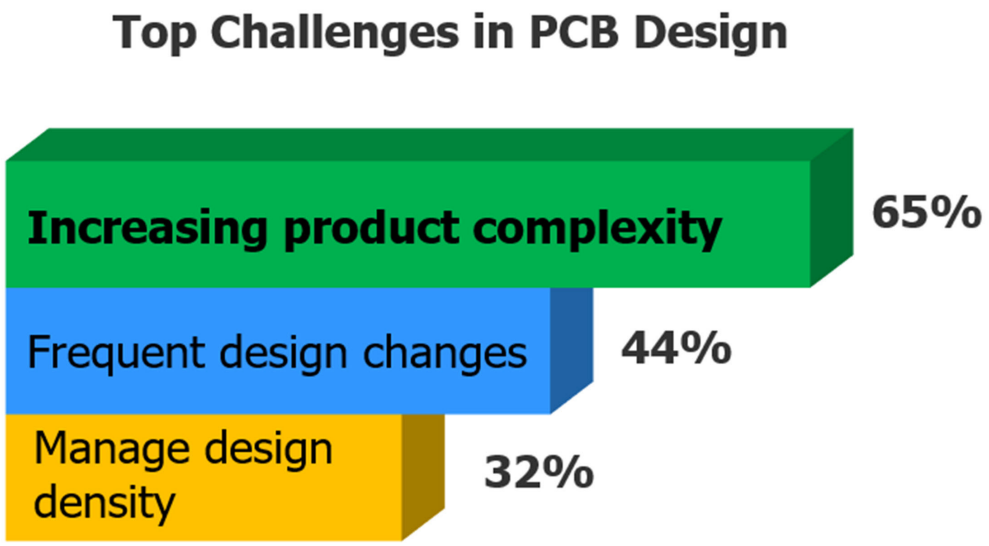

Figure 1: Top challenges in PCB design (Source: Aberdeen Group)

The Aberdeen Group's findings reinforce the criticality of ensuring that the schematic design is error-free throughout the product development process. This paper discusses how an efficient, fully automated, schematic review process can be an enabler for design teams to eliminate schematic design errors, thereby reducing costly respins and improving time to market.

MANUAL SCHEMATIC REVIEW – NO LONGER AN OPTION

Schematic capture is certainly not the most exciting or glamorous task within the product development process. In fact, many hardware engineers delegate the task to technicians within the team, providing hand drawings or PowerPoint representations of the circuit for the technician to interpret and enter. This delegation allows the hardware engineer to focus on other tasks, such as circuit optimization or lab testing, but it also increases the importance of properly verifying that the schematic has been captured correctly.

Just as a great building cannot be built on a weak foundation, a great product cannot be designed on a weak schematic. As design complexity increases and product development time decreases, the need for fully automated schematic verification becomes more important. Without proper schematic verification, there is significant potential for additional hardware respins, slower time to market, increased field returns, and poor product quality (Figure 2).

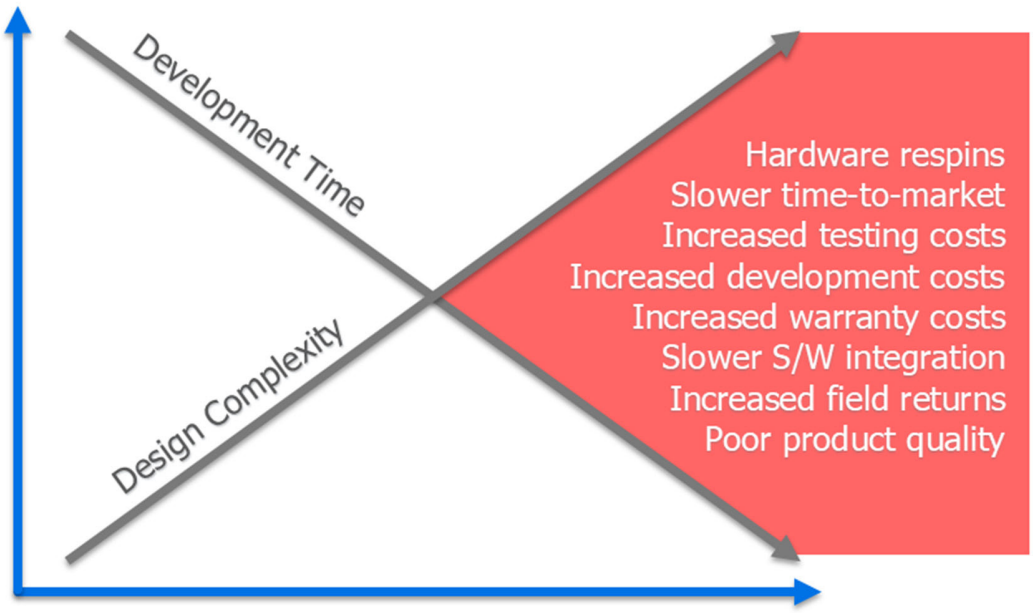

Figure 2: Impact of poor schematic verification as design complexity increases

During manual schematic review, teams typically focus on only the most common design issues including:

- Components not properly connected to power and/or ground
- Missing power
- Diodes oriented incorrectly
- Nets missing receiver
- Pin voltage mismatch (different voltage thresholds)
- Wrong board-to-board connectors
- Minor issues resulting in unnecessary delays, cost, and risk

While these are not complex issues, it is difficult, if not impossible, to visually find all occurrences of these issues in a complex design. And these are just the most common schematic issues. There are many more potential issues that a manual review simply cannot find.

FULLY AUTOMATED SCHEMATIC VERIFICATION

ECAD verification tools have historically focused on the layout and manufacturing aspects of the design, not the schematic. Given that 78% of all projects experience two or more respins, and that the root cause for many of the respins can be traced back to schematic design errors, the time has come for fully automated schematic verification. Eliminating schematic errors can result in significant cost- and time-savings, resulting in faster time-to-market, improved product quality, and lower risk (Figure 3).

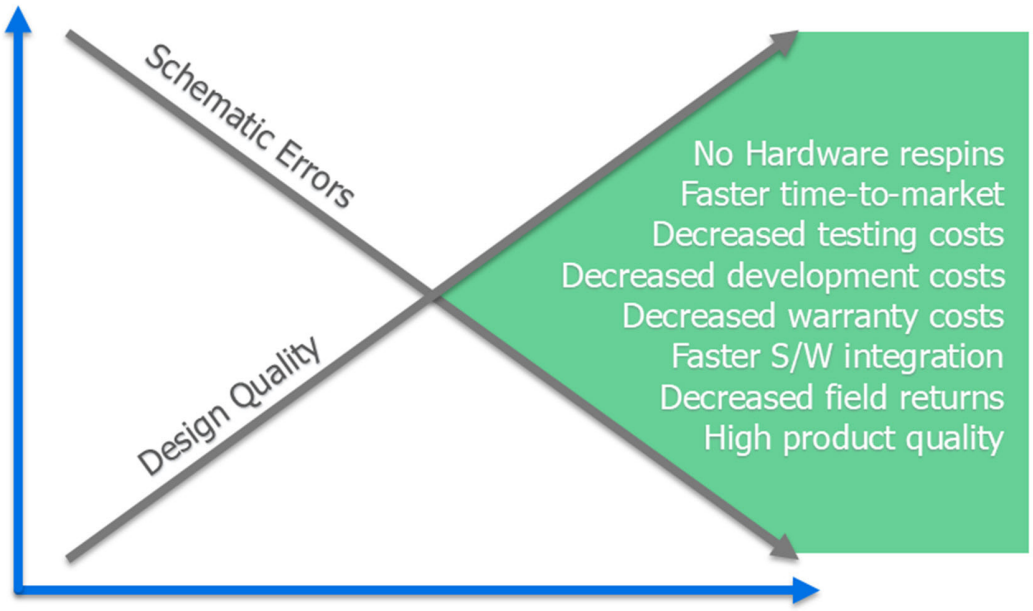

Figure 3: Impact of reduced schematic errors

By fully automating schematic verification to occur during schematic capture, rather than after, the development process shifts to the left, resulting in proven benefits such as reduced cycle time, lower costs, and the elimination of design spins (Figure 4).

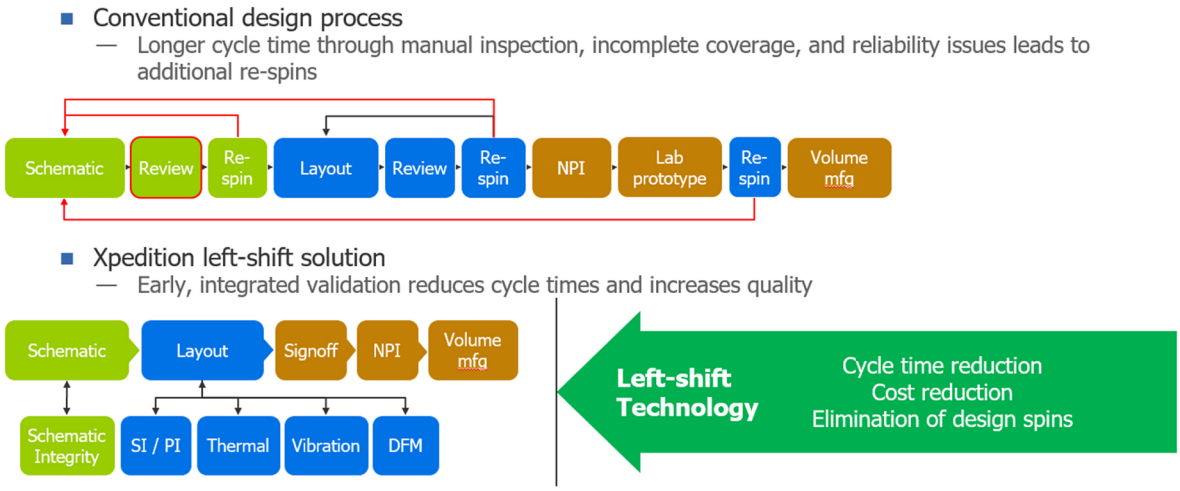

Figure 4: Left-shift technology

Using Xpedition® schematic integrity analysis, engineers can fully inspect all nets on a schematic using pre-defined checks and an extensive intelligent model component library. This automated schematic analysis can save design teams hundreds of hours of visual inspection and lab debug time. The checks execute rapidly in parallel with schematic capture, such that layout can commence with the highest confidence for first-pass success. The 125+ proprietary schematic integrity analysis checks are exhaustive, rapid, and power- and technology-aware. They are designed to identify both parametric errors and poor design practice and work with all major PCB design tools.

Key features of Xpedition schematic integrity analysis include:

- 125+ built-in automated checks
- 6 million+ intelligent models
- Support for the creation of custom device models
- Full inspection of 100% of a schematic's nets
- Support for multi-board interconnect analysis
- Easy setup and intuitive operation
- Intelligent post-processing results and reporting for tracking and audits
- Works with all major EDA tools
- No additional infrastructure required

Select examples of the schematic checks performed by Xpedition schematic integrity analysis include:

- Pin voltage parametric verification for maximum, minimum, and logic thresholds
- Bus flip errors (MSB to LSB, TX and RX errors)
- Full multi-board and backplane interface verification
- Pin function compatibility tests
- Symbol mismatch (to datasheet)
- Driver/receiver technology matching
- Diode orientation verification
- Driver/receiver function matching
- Power/ground/open collector/drain shorts
- Capacitor decoupling sufficiency checks
- Capacitor voltage derating (to user derating rules)
- Redundant resistors (on a net detection)
- Open collector/drain verification
- Poor design practice checks (i.e.: using pull-ups, pull-downs when needed...)
- Power/ground plane connection verification
- Component power checks
- Multiple or missing power supplies (on a net)

- Differential pin verification
- Unconnected nets or bus detection
- Off-board nets detection
- Overloaded pins identification
- Unconnected mandatory pins identification
- Nets missing driver
- Nets missing receiver

On average, Xpedition schematic integrity analysis performs 400,000 checks per design. An example of the results after performing Xpedition schematic integrity analysis on a schematic are show in Figure 5.

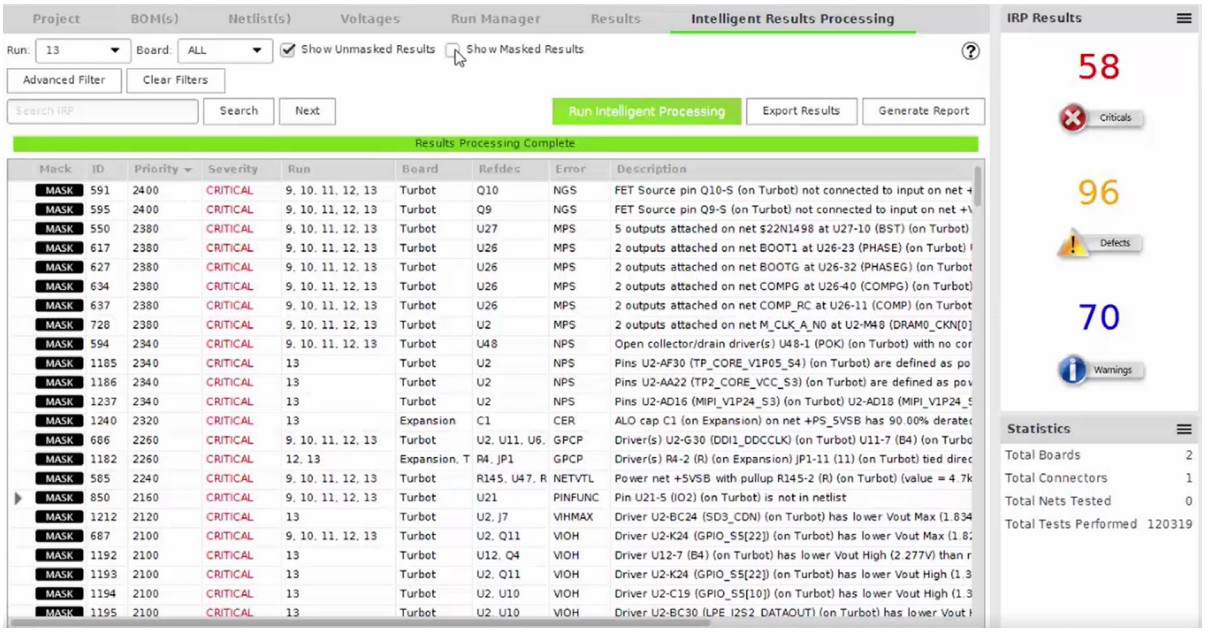

Figure 5: In this example, Xpedition schematic integrity analysis found 58 critical issues, 96 defects, and provided 70 warnings – far more than could ever be found with manual checking

SUMMARY

One of the primary goals of any product development team is to reduce the number of design respins before releasing a product to market. Given that the root cause of design respins is often schematic design error, a process that includes fully automated schematic verification can significantly mitigate the incidence of this costly issue. Xpedition schematic integrity analysis enables full inspection of all nets on a schematic using pre-defined checks and an extensive intelligent model component library.

Specifically, Xpedition schematic integrity analysis:

- Automates the detection of critical design errors
- Has been proven to eliminate 50% to 70% of design respins caused by schematic errors and marginalities
- Provides the confidence and assurance that design intent is implemented right the first time
- Eliminates many hours of manual review, reduces risk, and delivers a fast ROI with minimal training.

New designs can be modeled and continually analyzed to assure that last-minute design changes are fully assessed. Data from multiple board designs can also be integrated to perform system-level validation. Furthermore, schematic integrity analysis can be performed on designs after they have been released into the market to improve the quality of the electronic design, increase yield, and decrease product returns.

Today's complex designs no longer allow for manual schematic review and verification. Xpedition schematic integrity analysis provides fully automated schematic verification simultaneously with schematic capture. Unique technology ensures full inspection of all nets on a schematic resulting in fewer design spins and ensuring improved time to market.

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