# LEAN NPI WITH VALOR—CLOSING THE GAPS BETWEEN PCB LAYOUT DESIGN AND MANUFACTURING

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WHITEPAPER

Mentor Graphics®

PCB MANUFACTURING

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## INTRODUCTION

The Valor® NPI software from Mentor Graphics is a unique new product introduction (NPI) solution that seamlessly links printed circuit board (PCB) layout design and manufacturing processes and operations. Valor NPI enables the industry's first integrated, comprehensive, and automated workflow for PCB layout design, fabrication, and assembly and test. Layout designers and product-level NPI engineers can prepare and validate product models using embedded or concurrent design-for-manufacturing (DFM) analysis while they are working with the leading PCB layout design tools.

Implementing a Lean NPI flow facilitated by Valor NPI involves left-shifting DFM checks so they are concurrent with PCB layout design operations and generating an optimal product-model in ODB++ format for handoff to process-NPI. Our customers have been able to reduce design re-spins, improve overall product quality, and shorten their product delivery schedules using this Lean NPI product-to-process flow.

## NEW PRODUCT INTRODUCTION FOR PCBs

The success of a new electronic product is determined at the NPI stage. This critical stage is the transition from the PCB layout design domain, where the primary focus is creating the product model, to the manufacturing domain (fabrication, assembly and test), where the main focus is defining and running a suitable manufacturing process that results in high quality, lowest-cost production. NPI can be divided into two phases: the product phase and the process phase.

### THE PRODUCT-NPI PHASE

The first phase occurs between the domains of product-definition and manufacturing process definition where the PCB layout designer's product is validated as being compatible with the intended manufacturing processes (DFM validation).

### THE PROCESS-NPI PHASE

The second phase is where the precise manufacturing process for a particular product is defined, including the creation of all execution-ready documents and programs for use on the factory floor.

## PROBLEMS WITH THE TRADITIONAL NPI PROCESS

Almost every PCB program manager has problems when the PCB goes to manufacture. Many of these problems are associated with manufacturing processes or yields or problems with assembly of the PCBs that result in scrap or a lot of rework. When this happens, modifications have to be done and the product re-spun at the layout level to achieve a satisfactory match between the product and the intended manufacturing process.

During the product-NPI phase, the layout design of the product is handed off to the manufacturers for DFM analysis. The DFM engineers then send their analyses back to the layout designer to implement any recommended modifications to optimize the product model for manufacturing processes. There could


*The traditional NPI flow.*

be several iterations of the design itself before the designer approves it ready for manufacture, especially if there are errors on any of the drawings.

Traditionally, PCB layout designers produce many drawings and data packages to send for manufacture. These traditional drawings and data contain specifications and requirements that the assemblers and fabricators need to know to deliver the correct product. When sent as separate BOM, Gerber files, component position lists, drawings, netlists, and other formats of data, the manufacturing engineers have to go through many steps to recompile and rebuild the product model.

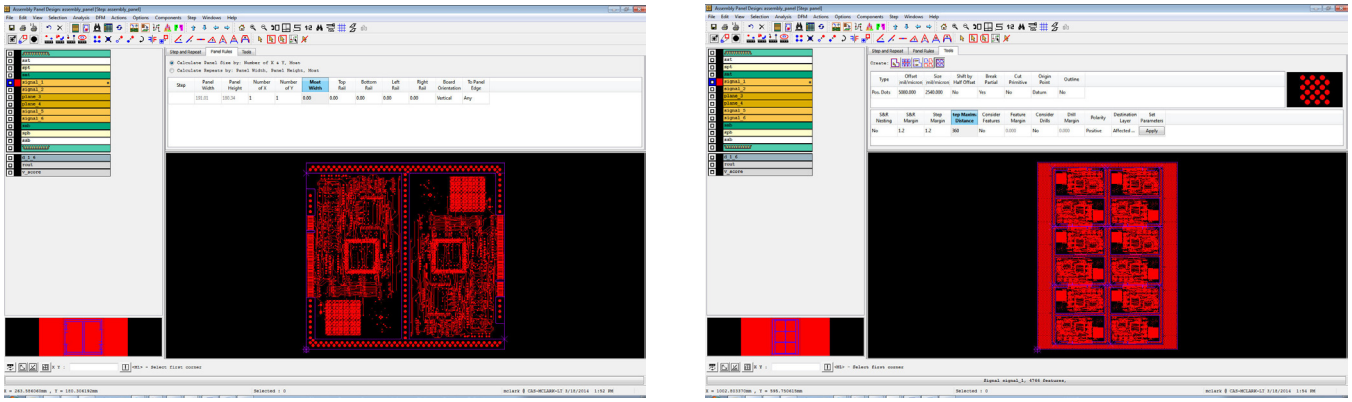
*"We send about 25 different format files as our standard data package: Gerber, drill files, netlists, etc. I'm sure each manufacturer uses about half of them but I'm never sure which half."*

When using traditional manufacturing data types, there's a lot of manipulation and recompilation of data that happens before PCB fabrication CAM and tooling. As Gerber data, Excellon tool drilling files, netlist files, and additional drawings are supplied to the PCB fabricators, many stages have to be performed before reaching the CAM and tooling stage. All of the data types need to be translated and then graphically verified. Individual layers of the PCB need to be registered and aligned. Any attributes needed for feature recognition need to be set. The layer buildup and material types need to be defined. The correct data for each manufacturing process needs to be extracted, and only then can the machine programming and tooling be generated.

Similarly, many stages are required before PCB assembly and test CAM processes. Again, the data has to be translated and verified. The top and bottom assembly layers need to be aligned. The BOM and netlist need to be integrated. Test point locations have to be input.

All of these stages for both fabrication and assembly/test are very time-consuming and introduce risk because of potential mistranslation of data and misunderstanding of drawings.

Once the PCB layout design is completed, then the designer or his manufacturing handoff colleague, using a combination of NPI engineering and mechanical drafting, with the input of the assembly panel guidelines provided by the assembly organization, PCB manufacturing data and the assembly panel drawing is produced and sent to the PCB fabricator.



*PCBs in an assembly panel (left), and assembly panels in a fabrication panel (right).*

An assembly panel usually contains one or more individual PCB circuits and is used solely for the assembly of the PCBs. The assembly panel is the fabrication supplier's deliverable that needs to comply with the assembler's requirements and specifications to suit the manufacturing processes and machines. The fabrication panel may contain many assembly panels, suiting the fabrication supplier's material sizes and capabilities.

The fabricators build assembly panel product models in data from the assembly panel drawing and then run further DFM analysis. Requests for more information to the layout designer may be sent to ensure they are working from a complete and correct model of the product. When this is done, the rebuilt final product-model is sent back to the design organization for review and approval. The approval of the assembly panel data is sent back to the PCB fabricator and only then can the fabrication tooling be created and the assembly panels fabricated.

Then begins a similar sequence with the assembly NPI engineer, during which the product model will be reintegrated on the assembly side, including this time integration of the BOM and approved vendors list (AVL). Following any necessary clarification and engineering change cycles, the assembly NPI engineer can then proceed with process preparation.

Traditionally, too much of the product-NPI work is "right-shifted" into the domain of the process engineers, which is highly inefficient.

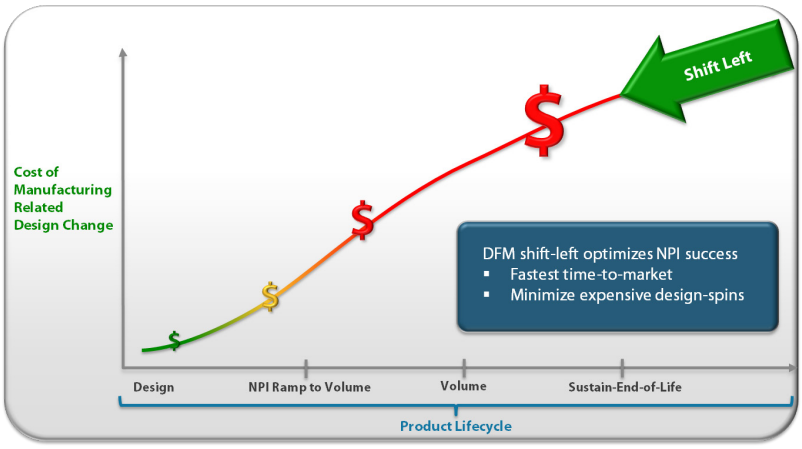
## BEST PRACTICE LEAN NPI—LEFT-SHIFTING DFM IN PRODUCT-NPI

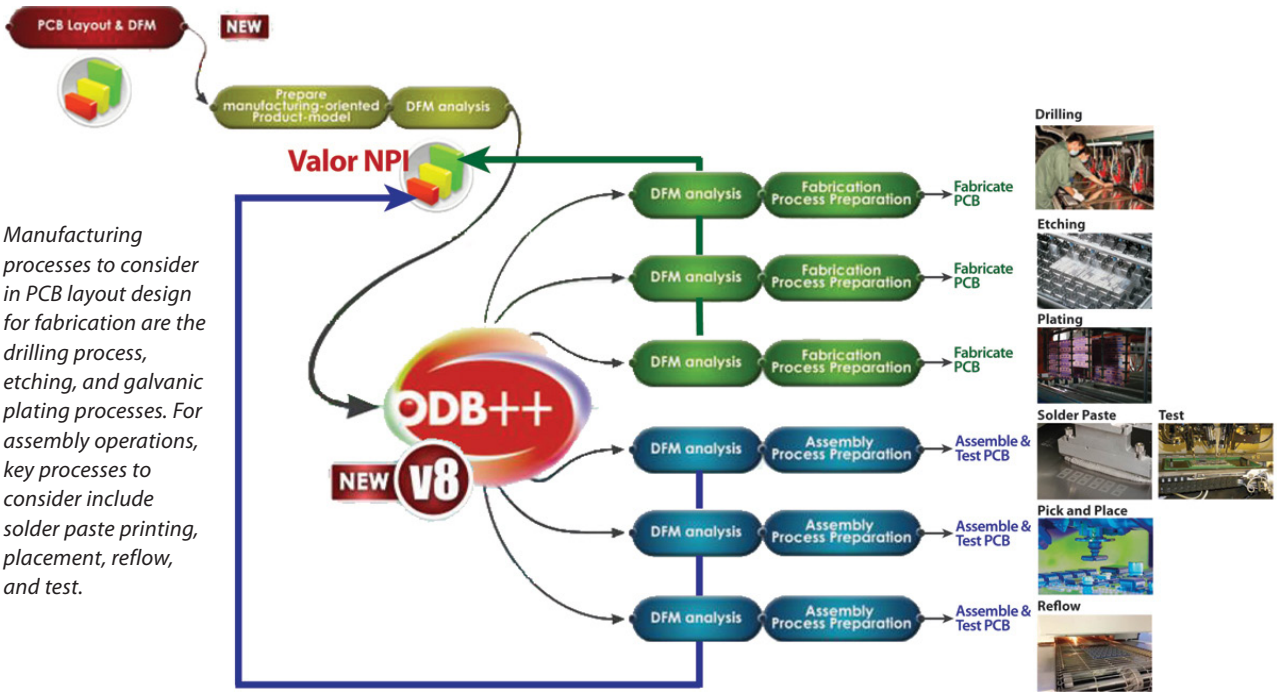
In contrast to the traditional approach, we propose using a Lean NPI workflow that scales easily across multiple manufacturers, accelerating the prototype phase as well as the transition into successful volume manufacturing.

Key to this alternative flow is "left shifting" the creation and management of DFM analysis rules so that these tasks become a unified product-NPI function within the design organization, running concurrently with PCB layout design operations.

In the recommended Lean NPI flow, the NPI engineers in fabrication and assembly, who manage their DFM rules in relation to their manufacturing processes, feed their rules to the NPI specialist at the design level, who manages them for use concurrently with the layout process.

*Identifying and implementing engineering changes early in the product lifecycle (left-shifting) can substantially lessen costs and save time when bringing a new product to the market.*



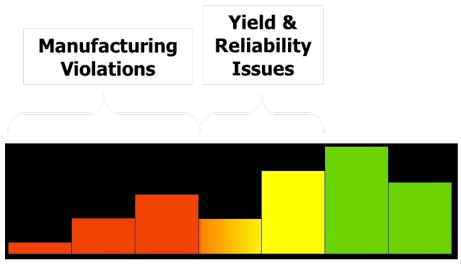



*Manufacturing processes to consider in PCB layout design for fabrication are the drilling process, etching, and galvanic plating processes. For assembly operations, key processes to consider include solder paste printing, placement, reflow, and test.*

Using DFM as part of the NPI flow vastly improves the handoff to manufacture and ensures the design is compatible with all the manufacturing processes. The rules used for DFM analysis are derived directly from the manufacturers' constraints and their capabilities. Holding regular review meetings with the manufacturers ensures that the DFM rules used at the design level are always up to date with the manufacturers' process-capabilities.

This Lean NPI flow is facilitated by the Mentor Graphics Valor NPI tool that enables dedicated DFM analysis during the PCB layout design process. It ensures that the design complies with the manufacturers' capabilities and that it doesn't cause any problems because of the constraints imposed by the intended manufacturing processes. Expensive and time-consuming problems experienced during PCB manufacturing can be avoided. Areas where the design can be improved are identified to ensure maximum yield from the manufacturer.

*DFM analysis results are not presented as "go/no-go" as they are with design-rules checking. Manufacturing process is all about percentage yield and degrees of quality and product-reliability. So the results are presented according to severity, from "cannot manufacture" to "fully OK," with opportunities to improve yield in the yellow zone between. For example, the yellow results might be OK for the prototype manufacturer, but would be a barrier to successful ramp-to-volume. Application of the rules enables the layout designer to manage the progress of the product all the way to volume production.*




With the latest version of Valor NPI, DFM analysis can be run concurrently at milestones during the PCB layout design. It is compatible with PCB design tools such as Mentor Graphics Xpedition® and PADS®, Cadence Allegro®, Zuken CR5000 and CR8000®, and Altium®. One-hundred and twenty DFM checks are embedded directly into the Xpedition xPCB Layout tool as part of the Xpedition designer's desktop. For the other design tools, DFM issues found can be automatically synchronized for quick resolution. All data file formats are supported; however, it is the latest version of ODB++ (open standard for intelligent design-to-manufacturing data transfer), that enables the comprehensive flow of critical structured data files between PCB layout design and PCB manufacturing disciplines.

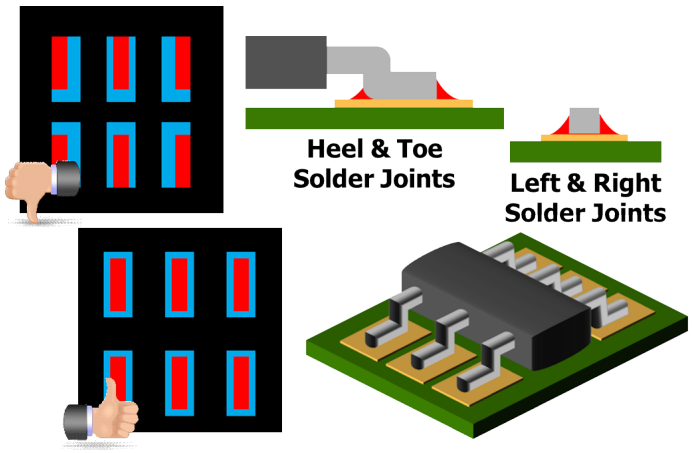
The Valor NPI engineering rule file (ERF) manages the rules that represent the manufacturers' processes. Each ERF contains all of the rules and process constraints that are then used to directly drive the DFM analysis. The Valor NPI ERF Manager provides complete control over all the rules required for successful fabrication, assembly and test of a PCB.

Valor NPI can run more than 700 different DFM checks on a design—more than half of which are dedicated to assembly and test DFM analysis. DFM analysis is performed using the Valor Parts Library (VPL), a dedicated library specifically to be used for assembly analysis and process preparation. The parts library contains more than 35 million manufacturers' part numbers where each has a VPL model associated. Each model is created using a traceable ISO 9001 process. Every VPL model carries the component body and pin-contact areas including the manufacturing tolerances of each. The pin-contact area defines where the component actually touches the PCB and the solder-joint is formed. Using VPL identifies issues that cannot be found using CAD libraries because they do not carry the same pin contact information, being purely for the copper pad layouts and placement outlines.

Valor NPI has a reporting function that enables creation of customized reports of the design at any point in the product-NPI flow. The reporting software interrogates the ODB++ data directly, extracting information on request. The DFM analysis results are contained in the ODB++ data, which means DFM results can be accessed by the reporting tool and a report can be generated of any DFM problems found with the design. A simple XML or HTML file is then generated that can be imported into third-party tools such as Microsoft® Office.

## IDENTIFYING PIN-TO-PAD MISMATCH

A common problem seen during assembly of PCBs is poor quality solder joints. Looking at the relationship between the device pin and the copper pad that it is going to be soldered to, there needs to be sufficient solder joint on the heel and toe of each component lead, as well as the left and right of each component lead. If these distances are in accordance with manufacturing process requirements, then there will be high-quality solder joints each time.




*Pin-to-pad mismatch is the number-one reason for unreliable solder joints.*

Ideally, the pin-to-pad relationship should provide sufficient copper land around the pin to ensure a high-quality

solder fillet during reflow. Pin-to-pad mismatch is the number one reason for unreliable solder joints. Using Valor NPI with VPL, these mismatches can be spotted at the design stage, long before the board goes through expensive assembly processing.

### IDENTIFYING PROBLEMS WITH COMPONENT SPACING

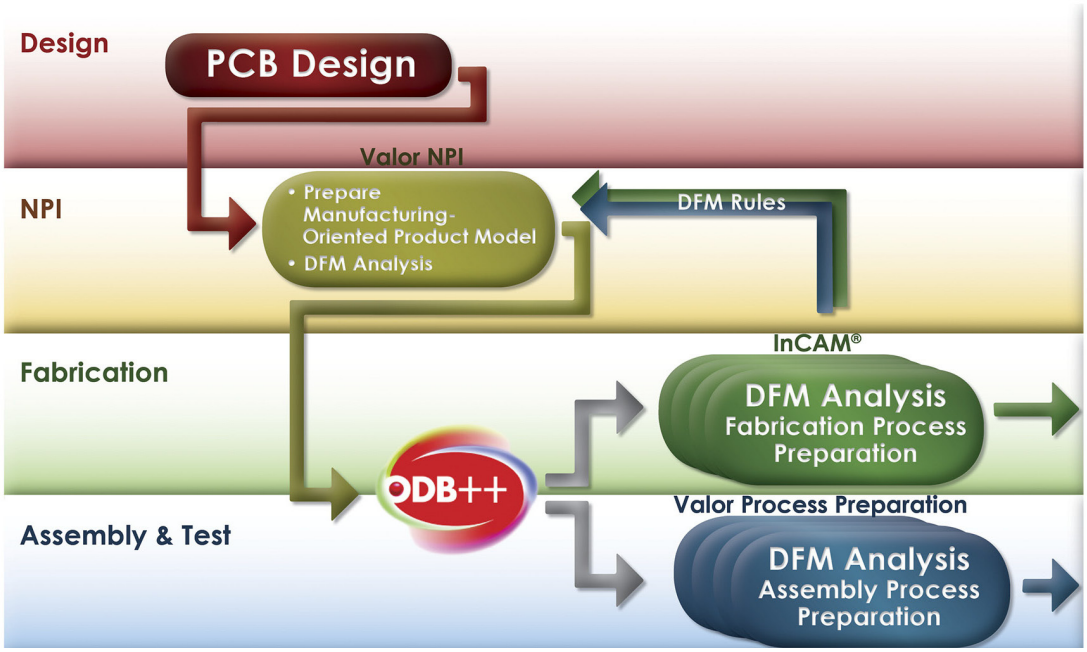
Although components look fine on the design, the relative proximity between the components highlighted can cause problems during the placement stage of the assembly process or problems if rework is required. Each component may have different spacing requirements caused by constraints of the pick-and-place machine. This needs to be taken into account when designing the PCB; and by running component-spacing DFM analysis, these problems can be identified very early.

Alternative parts, defined in the AVL, need to be taken into consideration so maximum supply-chain flexibility is achieved. These parts may be the same components in terms of their electrical characteristics but may come from different manufacturers with different part numbers. Valor NPI and VPL can be used to ensure that any combination of alternative parts can be used to manufacture a particular product. The analysis creates a composite component body that can be used for spacing DFM. The part's ability to be soldered also can be ensured by checking each part for sufficient copper land pattern for a satisfactory solder fillet.

## BEST-PRACTICE LEAN NPI—GENERATING THE OPTIMAL PRODUCT-MODEL FOR HANDOFF TO PROCESS-NPI

With the Lean NPI flow, the final manufacturing outputs are derived directly from the master ODB++ data that was used all along the way through the lean, integrated product- and process-NPI stages. Depending on the exact manufacturing machinery to be used, the data output can be modified to suit.

*In contrast to the traditional NPI flow characterized by cost increases, quality risks, and delays, a more-efficient lean NPI flow is possible today using Valor NPI embedded and/or concurrent DFM analysis with leading PCB layout design tools.*



In the best-practice Lean NPI flow, the manufacturing-level product model in ODB++ format includes a fully constructed and verified assembly panel in one structured data file. From this master product model file, combined with a defined manufacturing process definition, the manufacturing-process data can be automatically generated for fabrication, assembly, and test. This makes the NPI process much faster, while reducing the possibility for error and lowering the risk.

## SUMMARY

The best-practice Lean NPI flow uses enhanced, intelligent ODB++ product model data, concurrent DFM during the PCB design, and DFM rules that are derived directly from the manufacturer's rules and process constraints. Adopting all three of these practices will result in a Lean NPI flow.

This Lean NPI flow enables faster design and manufacture of PCBs at lower cost, while addressing the many issues that go along with using out-dated and localized design-to-manufacturing flows when a truly global approach is needed. PCB layout designers benefit from technology that integrates DFM into the design process more than ever before, and manufacturers benefit by being able to deliver higher value to their customers' design processes.

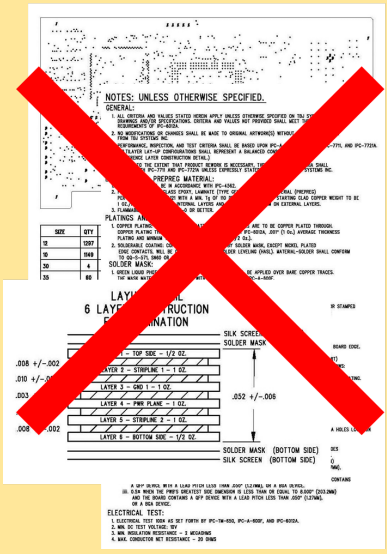
Companies that have implemented the Lean NPI flow experienced higher levels of product-quality assurance, enhanced supply-chain flexibility across multiple manufacturers, fewer unexpected delays in NPI, and fewer high-cost design-revision spins after the product is launched into manufacturing.

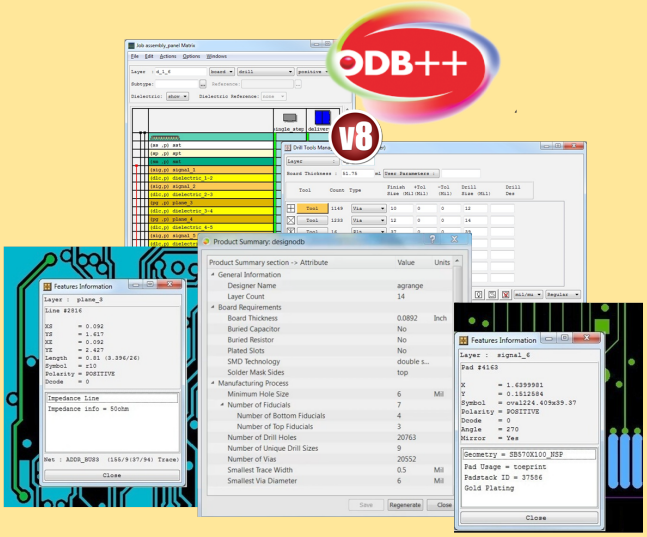
For more information on how using Valor NPI and implement a lean NPI workflow can benefit your company's PCB design and manufacturing, visit http://www.mentor.com/pcb/xpedition/pcb-npi

## WHAT IS AN ODB++ PRODUCT MODEL?

ODB++ is a complete PCB manufacturing exchange data format that contains all of the data required for defining a PCB product in manufacturing. It is an intelligent definition of an assembled PCB, including the bare board, a product model which defines exactly what is expected to be delivered back from the manufacturer. It enables direct import into process preparation without having to re-engineer or re-compile any of the data. Using ODB++ ensures that there is no misinterpretation of design intent and that the manufactured product is exactly what was designed. "ODB" stands for Open Data Base, with the format openly available to anyone who registers as a member of the ODB++ Solutions Alliance (www.odb-sa.com).

The ODB++ product model contains all the data the manufacturer needs to make the PCB. All of the fabrication requirements such as the graphical-definition of the layers or mechanical information, the underlying data represented in drawings such as the drill drawings, fabrication instructions, layer buildup definition, and also the information required for bare-board testing and automatic optical inspection are included. For the PCB assembly, all of the manufacturing information is included—the solder paste definitions, the component placements and rotations, the bill of materials (BOM) and the approved vendor list for alternative parts, as well as the ICT test-point locations. All this rich product model content is contained within a simple archive that can be sent to those in your manufacturing supply chain.




*When a complete lean product-NPI is done, the ODB++ product model is much more than just an alternative to Gerber. It delivers a complete definition of what has to be manufactured, including all of the information traditionally carried in paper or PDF documents, integrated into the structured data ready for immediate and automatic use by the next software tools in the flow.*

Within the ODB++ product model are the PCB Steps. Originating from the term "step and repeat," the ODB++ Step is a container for all the elements required for a PCB object. A Step can be a single PCB object, an assembly panel object, or a fabrication panel object containing a number of assembly panels.

It includes the PCB product matrix that defines all of the layers required for the PCB with their signal layers, power and ground layers or mixed layers, and the solder mask and solder paste layers…all listed in the correct order. Component layers are added for the top and bottom sides of the PCB, and all of the drill pairing information is included. Specific layers for routing and v-scoring information as well as documentation layers are included.

Because all of this information is included in ODB++, a build-up drawing is not needed to define the layer stack. All of the physical layers detail is included such as the legend layer used during the silk-screening process, the solder mask layers for both top and bottom sides of the board, as well as all of the copper layers required together with their thicknesses/weights and foil/laminate variations. This means that Gerber files, a listing of the layers, or any other readme files do not need to be sent that would traditionally be sent to the PCB manufacturers.

All of the drill-pair layer information is included, and for each one of those drill-pairs layers we have a drill tool layer that includes all of the drills needed for that drill pairing and includes the finished drill size as well as the type of hole,

whether it is plated or nonplated or maybe a via. This means there is no need to supply Excellon drill files, drill drawing, or any drill table to define the drilling information because it is self-contained in the ODB++ product model.

Often a netlist needs to be sent to PCB fabricators so they can perform bare-board tests. ODB++ contains netlist information. The netlist is generated directly from the PCB CAD system that contains all of the functional net names. ODB++ contains a second netlist derived directly from the copper features and the drill interconnects, and this netlist can be used to drive the bare-board test.

The component layers are included in the PCB product matrix, and they carry all the component placement information required for pick-and-place during assembly. ODB++ also includes the reference designators, along with *x* and *y* coordinates, rotations, and placement side. This removes the need for any separate assembly drawings, pick-and-place files, or assembly instructions as a way of conveying the product model into process-preparation.

As part of the assembly process for surface-mount devices, the solder paste aperture needs to be defined. In ODB++, it can be defined exactly for the solder-paste stencils for both top and bottom sides of the PCB.

The ODB++ product model also contains the BOM that includes reference designators, the manufacturer names, manufacturers' part numbers, and the quantities. In the case of an approved-vendor list, alternative manufacturer names and part numbers can be included if more than one manufactured part can be used. There is no need to send a separate BOM file to the assembly company, unless it has changed for any reason since the design was completed, in which case, it should be checked again through the product-NPI phase.

A well-constructed ODB++ product model replaces drawings traditionally sent for PCB manufacture. Instead of using legacy data, ODB++ enables the production engineer to go straight to process-NPI. Using ODB++, none of the product-model rebuild activity needs to happen, and fabrication, assembly and test process-NPI can begin straightaway.

## PROTECTING INTELLECTUAL PROPERTY WITH ODB++

ODB++ does not contain any greater level of "intellectual property" (IP) about a PCB design than the sum total of all the well-known legacy documents, files, and drawings that it replaces. However, it does present all that same content in a much more coherent and structured way. For designers concerned about the IP security of their product-models across the manufacturing supply chain, different ODB++ sub-models can be generated from the master product model in Valor NPI for different manufacturing disciplines. For example, for fabrication, the component-layers can be omitted and the net-names normalized into a simple numerical sequence; for assembly and test, the inner layers data and multilayer build structure can be omitted if desired.



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