# INTEGRATED VERIFICATION: A SHIFT-LEFT SOLUTION FOR A MORE EFFICIENT DESIGN FLOW

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# INTRODUCTION

## THE CHALLENGE – GETTING COMPLEX DESIGNS TO MARKET AS QUICKLY AS POSSIBLE

The rapidly increasing complexity of today's designs, combined with schedule pressure to deliver innovative products to market as quickly as possible, strains engineering resources to the limit, often to the point of breaking. As a result, 17% of all projects get canceled, and another 28% miss their target release date. Project health is suffering. A more efficient design flow is needed to better utilize available engineering resources, while keeping complex projects moving forward on schedule.

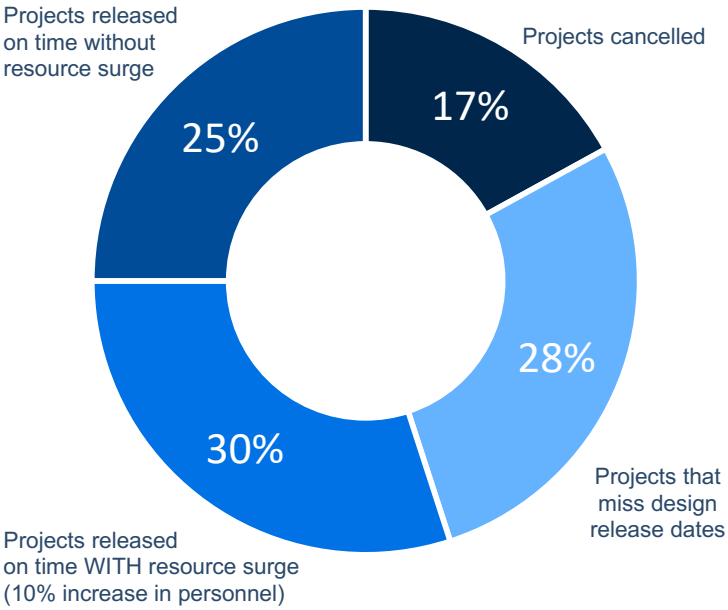



*Figure 1 – Poor Project Health*
*Source: Lifecycle Insights – September 2018*

The key to a more efficient design flow is the early detection and elimination of potential design issues. These potential issues can range from simple schematic errors allowed to propagate forward into layout, to complex mechanical issues, to issues impacting product testability and manufacturability. Identifying and fixing these potential issues as early in the process as possible avoids unnecessary schedule delays and costly design re-spins. It also frees up valuable engineering talent to move on to other projects.

# THE CONVENTIONAL DESIGN FLOW

The traditional project development flow (Fig. 2) is inefficient and fraught with pitfalls. It relies far too heavily on manual reviews and costly prototypes. Verification of each design phase occurs far too late in the process. Valuable engineering resources are spent debugging errors in the lab that should have been caught during schematic entry. Errors uncovered this late in the game result in costly re-spins, that once again follow the same inefficient, error prone, manual review process.

As a result of this conventional process flow, the typical project goes through 2.9 re-spins, with an average schedule hit of 8.5 days and a cost of $44,000 per re-spin (Source: Lifecycle Insights – September 2018). For high-performance designs, the costs are often much higher. Due to the complexities of modern designs, these delays and added costs are unpredictable and project managers tend to bake them into their schedules and budgets. This conventional approach wastes time, talent, materials and puts projects at risk for cancelation.

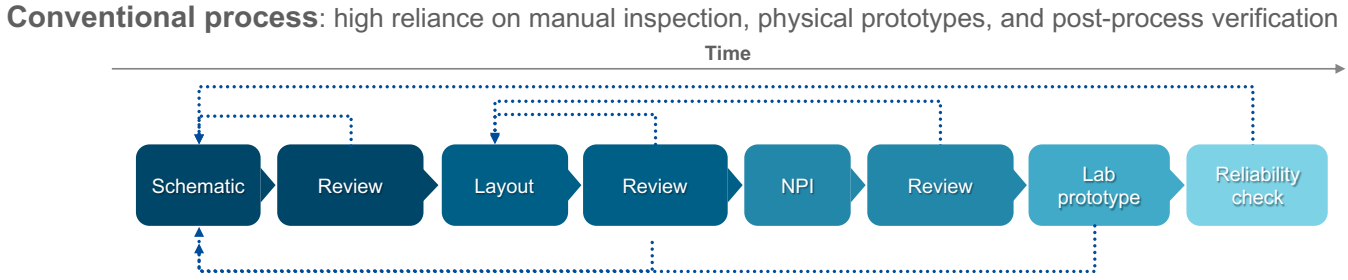



*Figure 2 – The Conventional Project Development Flow*

## THE SHIFT-LEFT APPROACH TO INTEGRATED DESIGN VERIFICATION

In order to eliminate the inefficiencies of the conventional design flow, a "shift-left" approach is desired that integrates verification as early as possible in the design process (Fig. 3). This means catching errors and potential issues at the source, before they can propagate forward into subsequent phases of the project. Schematic errors should be caught during schematic entry, not in the lab after building costly prototypes and hundreds of hours of debug time. Automated schematic integrity analysis should be employed to eliminate the reliance on manual, visual schematic reviews.

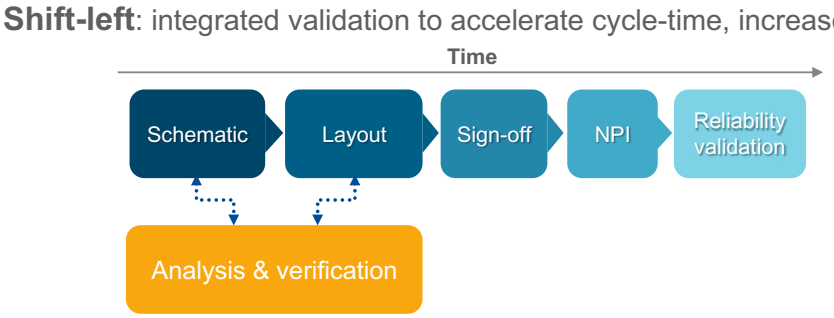
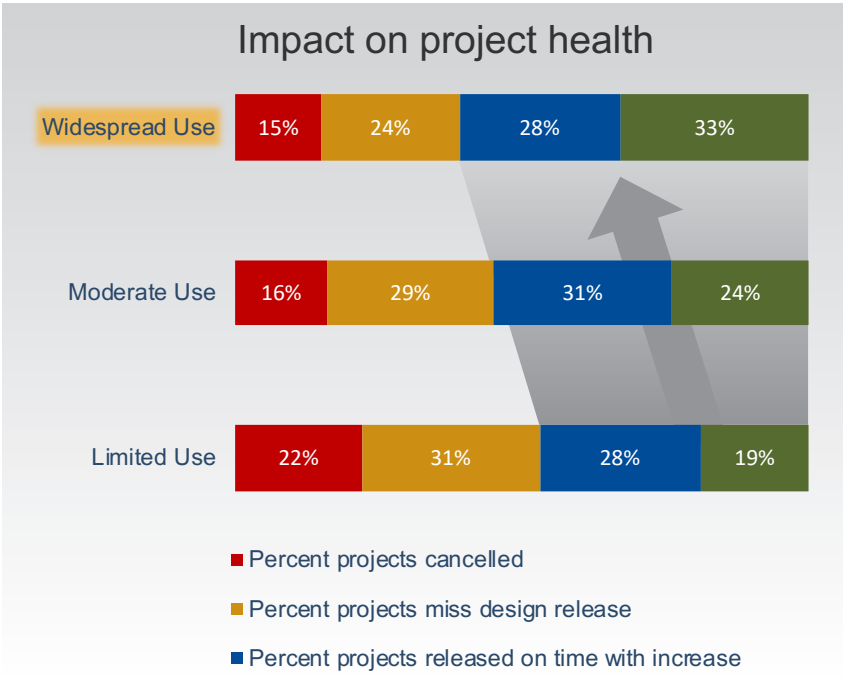



*Figure 3 – A Shift-Left Approach for Integrating Verification into the Design Process*

Routing constraints for signal and power integrity, as well as design for test constraints should be specified during schematic capture, not shoe-horned in at the layout phase. Signal and power integrity, EMI compliance, thermal analysis and vibration analysis should all be validated during the layout process.

## THE COST VS. REWARD BENEFIT OF INTEGRATED VERIFICATION

Integrating verification early in the process does not come for free. Time and effort are required to develop models, run simulations and interpret the results. However, an integrated tool environment minimizes the complexity and overhead of adding verification to the design flow. The effort expended early in the process saves hundreds of hours debugging issues using physical prototypes, with the added benefit that issues discovered during the schematic and layout phases are easily corrected without the need for costly re-spins.




A recent survey by Lifecycle Insights shows that time spent up front, on verification during the design phase, is time well spent (Fig. 4). The result is a more efficient process with greater coverage than possible using a conventional approach that relies on manual peer reviews. The increased time spent during design and verification analysis reduces the time spent testing and debugging physical prototypes, leading to improved project health. The same study shows that widespread use of design

*Figure 4 –*
*The Impact of Verification on Design Cycle Time*
*Source: Lifecycle Insights – September 2018*

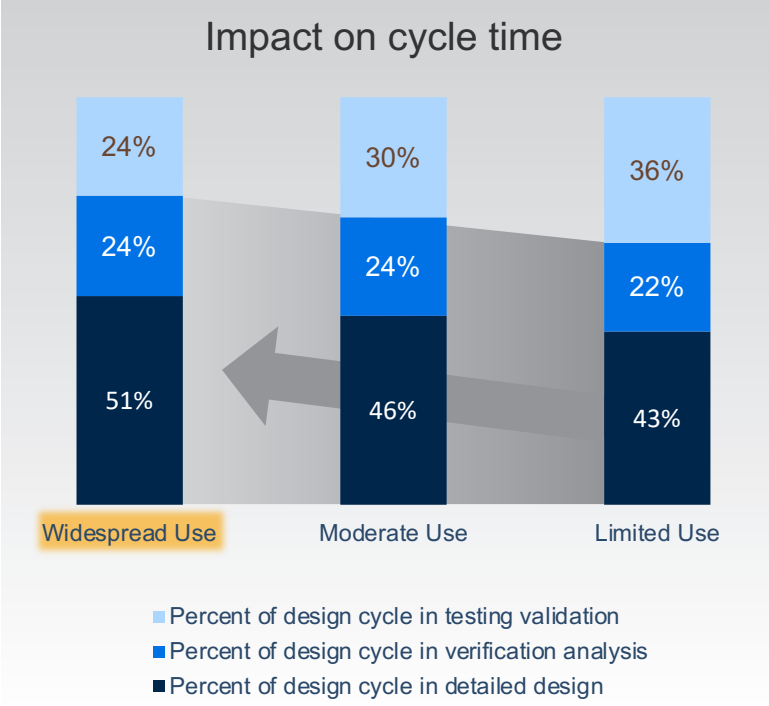



*Figure 5 – The Impact of Verification on Project Health*
*Source: Lifecycle Insights – September 2018*

verification substantially improves the chances that a project will release on schedule and reduces the risk of project cancelation (Fig. 5)

> *"Our most recent research shows that the broad use of analysis and verification throughout the design phase directly supports engineering management's efforts to compress the design cycle while improving board systems quality*
> *– Chad Jackson, President & Principal Analyst, Lifecycle Insights*

The integrated verification flow provides substantial value for both engineering and management. Engineering benefits from a more thorough, automated process that improves coverage, catches errors and identifies potential issues at a point where they are easily corrected. Management benefits by eliminating re-spins that add unpredictable schedule delays and cost over runs. The ultimate goal should be an all-inclusive, multi-dimensional verification process that reduces reliance on both manual reviews and manual debugging of physical prototypes (Fig. 6).

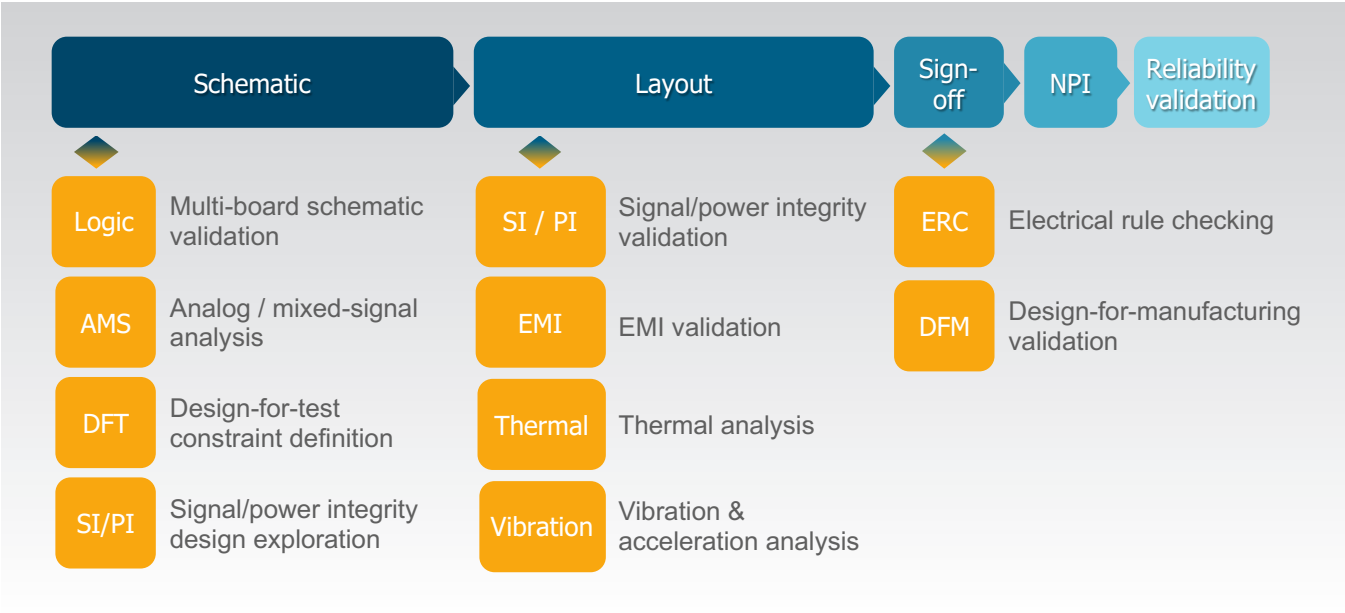



*Figure 6 – An Inclusive Multi-Dimensional Verification Process*

## THE KEY COMPONENTS OF A SHIFT-LEFT APPROACH TO CREATING AN INTEGRATED VERIFICATION DESIGN FLOW

The shift-left solution integrates a broad range of analysis and verification tools during the schematic and layout phases of the project. These tools are aimed at non-specialist PCB design engineers and layout designers and allow them to work within their familiar authoring environments to identify problems early in the design.

An integrated verification flow starts at the source – the schematic. Errors caught and fixed here have the greatest impact on the rest of the process. They are also, traditionally, the ones most likely to slip through the cracks and go undetected using conventional manual review processes. Relying on a "second set of eyes" to review a complex design with multiple PCBs and thousands of components is time consuming, limited in scope and error-prone. It adds time to the schedule, consumes valuable engineering talent and still allows many simple, easily fixed schematic errors to be passed through to layout and subsequently hard-wired into physical prototypes.

Automated schematic integrity analysis replaces the manual review process. It enables full inspection of all nets in the design, for both single and multi-board designs, using pre-defined checks for common schematic errors and an intelligent component model library. The analysis is performed in parallel with schematic entry and eliminates most common schematic errors before layout starts. The design checks are power and technology aware. Common checks should include missing power and ground connections, incorrect diode orientation, missing or redundant pull-up and pull-down resistors, capacitor voltage derating, nets missing a driver or receiver, driver/receiver technology matching, board-to-board connectivity, bus flip errors (MSB to LSB), etc. Replacing the manual review process with an automated one results in greater coverage and much higher probability of entering layout with a schematic that will provide first-pass success.

Testability analysis should also occur during schematic entry, prior to layout. The goal is to move testability analysis to the left in the design flow and to automate the process. The design is analyzed, test point requirements are identified and passed to layout as constraints. The result is fewer errors due to insufficient test coverage, a quicker and smoother handoff to manufacturing with more efficient and cost effective test processes.

Signal integrity, power integrity and analog/mixed signal simulations and analysis should also take place during the schematic phase of the design. This allows the designer to develop a set of placement, routing and PDN constraints that meet the target design requirements. As with the test point requirements, these constraints are passed forward to layout.

During layout, signal integrity analysis is performed on all critical nets to ensure both signal quality and timing requirements are within spec. Power integrity analysis should include both DC drop analysis to identify excessive voltage drops and high current densities, as well as AC power plane analysis to optimize capacitor selection and placement.

As component placement is progressing, EMI validation, thermal analysis, vibration/acceleration and manufacturability analysis should all be performed to quickly identify and correct any potential issues. In the traditional design flow, these issues would not be discovered until physical testing in an EMI, thermal or HALT test chamber. If they are not caught during layout, issues that impact the mechanical integrity of the design are usually the most expensive and time consuming to fix. Such issues often require board re-spins and tooling changes to correct. Simulations during layout greatly increased the likelihood of first-pass success.

A post layout sign-off phase should include both electrical rule checking and design-for-manufacturing validation. In the conventional design flow, validation of the electrical performance of a design is often done by visual inspection by manually scanning through multiple PCB layers for ground return paths, potential noise sources and other layout related problems. Again, this is a process that should be automated by running a full board verification against a set of pre-defined rules. Finally, design-for-manufacturability verification should be performed to ensure the cost effective manufacturability of the final product. This should be a comprehensive analysis covering the fabrication, assembly and test of standard PCBs, rigid-flex and multi-board designs.

The goal of the shift-left approach is the same in all cases - to move as much verification as possible as early in the design cycle as permissible, while also automating the analysis to provide the highest possible degree of coverage. Identifying and correcting issues at the source eliminates time consuming debug efforts and costly re-spins. The conventional design flow is frustratingly unpredictable. It relies far too much on manual visual design checks that allow far too many errors to propagate forward to the next step in the process. The shift-left automated verification flow catches errors and identifies potential issues early in the process where they are quickly and economically corrected. It is a more efficient process that provides more predictable results, eliminates design re-spins and yields higher quality products in less time.

## WHAT DOES THIS MEAN FOR ME?

### AS A DESIGN AUTHOR (DESIGN ENGINEER OR LAYOUT DESIGNER)…

This verification strategy feels like additional process and tool steps to learn and execute, on top of an already-stressed workload. Tool integration within the authoring environment improves ease of use and minimizes the extra steps and the learning curve often associated with verification tools. In addition, automated verification checks eliminate manual peer reviews, and increase coverage so errors don't slip through the cracks. A little extra time spent verifying a design can result in first-pass success, minimizing lab debug time, and eliminating re-spin interrupts once I've moved on to the next project.

### AS AN ANALYSIS SPECIALIST…

This approach seems to shift my job into the hands of design authors. In reality, it ensures that designs are higher quality when they reach me, enabling me to focus on the more critical second-order problems in a design, while also enabling me to dedicate more time to the bleeding edge of what's coming next, from advanced signaling protocols to new manufacturing technologies.

### AS AN ENGINEERING PROJECT MANAGER…

Today, I ensure that a design comes out 'on time' by baking extra time into the schedule for manual reviews, re-spins and re-work. A shift-left process minimizes the bottleneck incurred with specialist reviews, and eliminates re-spins to bring projects in ahead of schedule. It also minimizes risk associated with higher design complexities, where never-before-seen problems have the potential to dramatically extend project timelines.

### AS AN ENGINEERING EXECUTIVE…

I know a smooth new product introduction process is critical for first-to-market releases. A shift-left methodology enables my engineering team to minimize risk by significantly reducing time and cost during design and prototyping, while at the same time increasing the quality of the end product.

## THE TOOLS TO IMPLEMENT A SHIFT-LEFT AUTOMATED VERIFICATION DESIGN FLOW

With the increasing complexities of advanced systems design, and competitive threats in delivering innovative products to market faster, engineering management needs to seek and adopt new technologies to succeed in today's global economy. There are several point tools available in the market to address some of the specific design challenges mentioned in this paper, however, what's needed for a shift-left methodology is a fully-inclusive system design platform for upfront design analysis and verification. Mentor, a Siemens business, is the first electronic design software company with a broad portfolio of proven technologies to enable "shift-left" design verification. The fully-integrated Xpedition® verification platform for single and multi-board PCB system design includes automated schematic integrity analysis with built-in automated design checks and an extensive library of intelligent models. Testability analysis, automated component modeling for vibration analysis, DC voltage drop analysis for rigid-flex and multi-board designs, as well as concurrent DFM analysis during layout, are additional technologies integrated within the authoring environment for easier, faster validation. The benefits of this new multi-dimensional verification platform are the reduction of costly design re-spins, improved time-to-market for new products, and the development of higher quality products with fewer defects.

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